Intel® Desktop Board D810E2CB

Technical Product Specification

January 2001

Order Number A44673-001

The Intel® Desktop Board D810E2CB may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D810E2CB Specification Update.

Revision History

Revision	Revision History	Date
001	First release of the Intel® Desktop Board D810E2CB Technical Product Specification.	January 2001

This product specification applies to only standard D810E2CB boards with BIOS identifier CB81010A.86A.

Changes to this specification will be published in the Intel® Desktop Board D810E2CB Specification Update before being incorporated into a revision of this document.

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT.

Intel Corporation may have patents or pending patent applications, trademarks, copyrights, or other intellectual property rights that relate to the presented subject matter. The furnishing of documents and other materials and information does not provide any license, express or implied, by estoppel or otherwise, to any such patents, trademarks, copyrights, or other intellectual property rights.

Intel products are not intended for use in medical, life saving, or life sustaining applications or for any other application in which the failure of the Intel product could create a situation where personal injury or death may occur.

Intel may make changes to specifications and product descriptions at any time, without notice.

The D810E2CB board may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 5937
Denver, CO 80217-9808

or call in North America 1-800-548-4725, Europe 44-0-1793-431-155, France 44-0-1793-421-777, Germany 44-0-1793-421-333, other Countries 708-296-9333.

† Third-party brands and names are the property of their respective owners.

Copyright © 2001, Intel Corporation. All rights reserved.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the D810E2CB desktop board. It describes the standard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the D810E2CB board and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on this board
2	A map of the resources of the board
3	The features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, and POST codes

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions which, if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the D810E2CB board, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
GB	Gigabyte (1,073,741,824 bytes)
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
†	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

Contents

Figures

Tables

1 Product Description

What This Chapter Contains

1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the D810E2CB board's major features.

Table 1. Feature Summary

Form Factor	FlexATX (9.00 inches by 7.50 inches)
Processor	Support for either an: • Intel® Pentium® III processor with 256 KB L2 cache (in an FCPGA package) • Intel® Celeron™ processor with 128 KB L2 cache (in a PGA package)
Memory	• Two 168-pin dual inline memory module (DIMM) sockets • Supports up to 512 MB of 100 MHz non-ECC synchronous DRAM (SDRAM) • Support for serial presence detect (SPD) and non-SPD DIMMs
Chipset	Intel® 810E chipset, consisting of: • Intel® 82810E Graphics/Memory Controller Hub (GMCH) • Intel® 82801BA I/O Controller Hub (ICH2) • SST 49LF004A 4 Mbit Firmware Hub (FWH)
Direct AGP Video	• Intel 82810E GMCH • VGA port connector on back panel
Audio	Audio Codec '97 (AC'97) compatible audio subsystem, consisting of the following: • Intel 82801BA ICH2 (AC link output) • CS4201 analog codec
I/O Control	LPC47M102 Low Pin Count (LPC) I/O controller
Peripheral Interfaces	• Four universal serial bus (USB) ports (two back panel, two front panel) • Two IDE interfaces with Ultra DMA, ATA-66/100 support • One diskette drive interface • One serial port • One parallel port • PS/2† keyboard and mouse ports
Expansion Capabilities	Two PCI-bus add-in card connectors
BIOS	• Intel/AMI BIOS stored in an SST 49LF004A 4 Mbit firmware hub (FWH) • Support for Advanced Configuration and Power Interface (ACPI), Advanced Power Management (APM), Plug and Play, and SMBIOS
Instantly Available PC	• Support for *PCI Local Bus Specification*, Revision 2.2 • Suspend-to-RAM support • Wake from USB ports

NOTE

The D810E2CB board is designed to support only USB-aware operating systems.

For information about	Refer to
The board's compliance level with ACPI, APM, Plug and Play, and SMBIOS	Table 3, page 16

1.1.2 Manufacturing Options

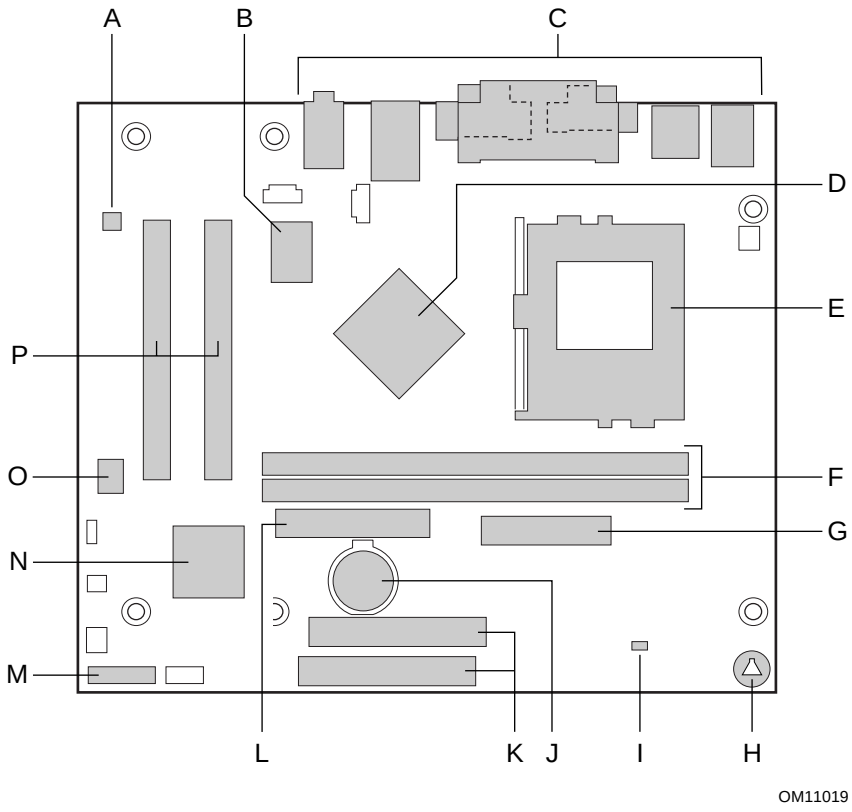
Table 2 describes the D810E2CB board's manufacturing options. Not every manufacturing option is available in all marketing channels. Please contact your Intel representative to determine which manufacturing options are available to you.

Table 2. Manufacturing Options

LAN	Intel® 82562ET 10/100 Mbit/sec Platform LAN Connect (PLC) device
Hardware monitor component	Hardware monitor component features include: • Voltage sense to detect out of range power supply voltages • Thermal sense to detect out of range thermal values

1.1.3 D810E2CB Board Layout

Figure 1 shows the location of the major components on the D810E2CB board.



A	CS4201 Audio Codec	I	Hardware monitor
B	SMSC LPC47M102 I/O Controller	J	Battery
C	Back panel connectors	K	IDE connectors
D	Intel 82810E GMCH (Graphics/Memory Controller Hub)	L	Diskette drive connector
E	Processor socket	M	Front panel connector
F	DIMM sockets	N	Intel 82801BA ICH2 (I/O Controller Hub)
G	Power connector	O	SST 49LF004A 4M Mbit Firmware Hub
H	Speaker	P	PCI bus add-in card connectors

Figure 1. D810E2CB Board Components

1.1.4 Block Diagram

Figure 2 is a block diagram of the major functional areas of the D810E2CB board.

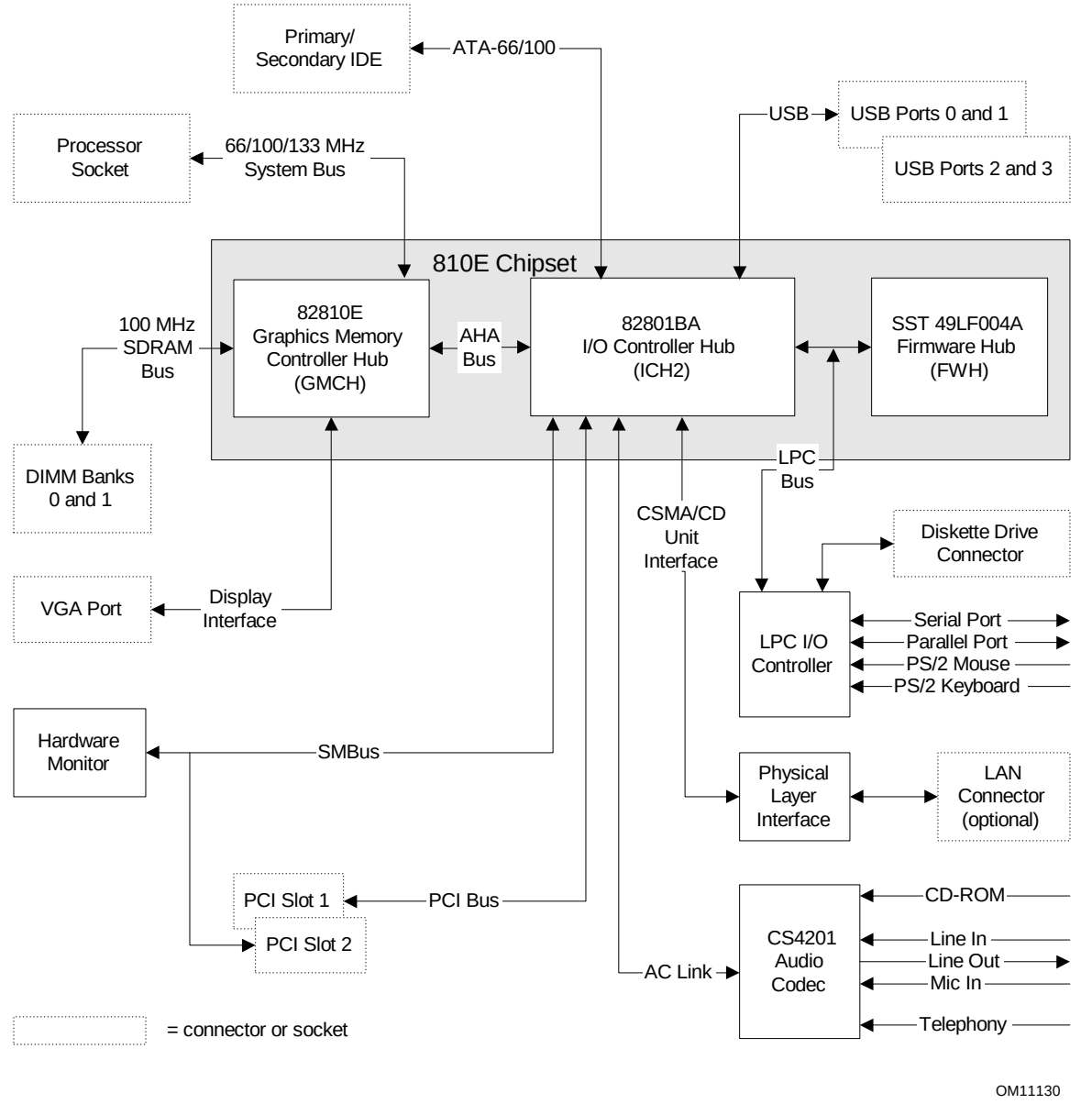


Figure 2. Block Diagram

1.2 Online Support

To find information about…	Visit this World Wide Web site:
Intel's D810E2CB board under "Product Info" or "Customer Support"	http://www.intel.com/design/motherbd http://support.intel.com/support/motherboards/desktop
Processor data sheets	http://www.intel.com/design/litcentr
Proper date access in systems with Intel® motherboards	http://support.intel.com/support/year2000
ICH2 addressing	http://developer.intel.com/design/chipsets/datashts
Custom splash screens	http://intel.com/design/motherbd/gen_indx.htm
Audio software and utilities	http://www.intel.com/design/motherbd
LAN software and drivers	http://www.intel.com/design/motherbd

1.3 Design Specifications

Table 3 lists the specifications applicable to the D810E2CB board.

Table 3. Specifications

Reference Name	Specification Title	Version, Revision Date, and Ownership	This specification is available from:
AC '97	*Audio Codec '97*	Version 2.1, May 1998, Intel Corporation.	ftp://download.intel.com/ pc-supp/platform/ac97
ACPI	*Advanced Configuration and Power Interface Specification*	Version 1.0b, July 1, 1998, Intel Corporation, Microsoft Corporation, and Toshiba Corporation.	http://www.teleport.com/~acpi/
AGP	*Accelerated Graphics Port Interface Specification* (2X only)	Version 2.0, May 4, 1998, Intel Corporation.	the Accelerated Graphics Implementers Forum at: http://www.agpforum.org/
AMI BIOS	*American Megatrends BIOS Specification*	AMIBIOS 99, 1999 American Megatrends, Inc.	http://www.amibios.com, or http://www.ami.com/download/ amibios99.pdf
APM	*Advanced Power Management Specification*	Version 1.2, February 1996, Intel Corporation and Microsoft Corporation.	http://www.microsoft.com/hwdev/busbios/amp_12.htm
ATA-3	*Information Technology - AT Attachment-3 Interface, X3T10/2008D*	Version 6, October 1998, ASC X3T10.	ATA Anonymous FTP Site: ftp://www.dt.wdc.com/ata/ ata-3/

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	This specification is available from:
ATAPI	*Information Technology AT Attachment with Packet Interface Extensions T13/1153D*	Version 18, August 19, 1998, Contact: T13 Chair, Seagate Technology.	T13 Anonymous FTP Site: ftp://fission.dt.wdc.com/x3t13/project/d1153r18.pdf
ATX	*ATX Specification*	Version 2.01, February 1997, Intel Corporation.	http://developer.intel.com/design/motherbd/atx.htm
El Torito	*Bootable CD-ROM format specification*	Version 1.0, January 25, 1995, Phoenix Technologies Ltd. and IBM Corporation.	the Phoenix Web site at: http://www.ptltd.com/techs/specs.html
FlexATX	FlexATX Addendum to the microATX Specification, Version 1.0	Version 1.0 March 1999, Intel Corporation.	http://www.teleport.com/~ffsupprt/spec/FlexATXaddn1_01.pdf
LPC	*Low Pin Count Interface Specification*	Version 1.0, September 29, 1997, Intel Corporation.	http://www.intel.com/design/chipsets/industry/lpc.htm
MicroATX	*microATX Motherboard Interface Specification*	Version 1.0, December 1997, Intel Corporation.	http://www.teleport.com/~ffsupprt/spec/
	SFX Power Supply Design Guide	Version 1.0, December 1997, Intel Corporation.	http://www.teleport.com/~ffsupprt/spec/microatx/sfx11_ps.pdf
PCI	*PCI Local Bus Specification*	Version 2.2, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
	PCI Bus Power Management Interface Specification	Version 1.1, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
Plug and Play	*Plug and Play BIOS Specification*	Version 1.0a, May 5, 1994, Compaq Computer Corp., Phoenix Technologies Ltd., and Intel Corporation.	ftp://download.intel.com/ial/wfm/bio10a.pdf
SDRAM DIMMs (64- and 72-bit)	*PC SDRAM Unbuffered DIMM Specification*	Version 1.0, February 1998, Intel Corporation.	http://www.intel.com/technology/memory/
	PC SDRAM DIMM Specification	Version 1.5, November 1997, Intel Corporation.	http://www.intel.com/technology/memory/
	PC Serial Presence Detect (SPD) Specification	Version 1.2A, December 1997, Intel Corporation.	http://www.intel.com/technology/memory/

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	This specification is available from:
SMBIOS	*System Management BIOS*	Version 2.3.1, August 12, 1998, Award Software International Inc., Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Limited, American Megatrends Inc., SystemSoft Corporation, and Compaq Computer Corporation.	http://developer.intel.com/ial/wfm/wfm20/design/smbios/index.htm
UHCI	*Universal Host Controller Interface Design Guide*	Version 1.1, March 1996, Intel Corporation.	http://www.usb.org/developers
USB	*Universal Serial Bus Specification*	Version 1.1, September 23, 1998, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, and NEC.	http://www.usb.org/developers
WfM	*Wired for Management Baseline*	Version 2.0, December 18, 1998, Intel Corporation.	http://developer.intel.com/ial/WfM/wfmspecs.htm

1.4 Processor

CAUTION

The D810E2CB board supports processors that draw a maximum of 22 A. Using a processor that draws more than 22 A can damage the processor, the board, and the power supply. See the processor's data sheet for current usage requirements.

CAUTION

Before installing or removing the processor, make sure that AC power has been removed by unplugging the power cord from the computer. Failure to do so could damage the processor and the board.

The D810E2CB board supports either an Intel Pentium III processor (FCPGA package), or an Intel Celeron processor (PGA package) as shown in Table 4. The system bus frequency is automatically selected.

Table 4. Supported Processors

Processor Type	Processor Designation	System Bus Frequency	L2 Cache Size
Pentium III processors	500E, 550E, 600E, 650, 700, 750, 800, and 850 MHz	100 MHz	256 KB
	533B, 600EB, 667, 733, 800EB, 866, and 933 MHz	133 MHz	256 KB
	1.0B GHz	133 MHz	256 KB
Celeron processors	800 MHz	100 MHz	128 KB
	400, 433, 466, 500, 533, 533A, 566A, 600, 633, 667, 700, 733, and 766 MHz	66 MHz	128 KB

All supported onboard memory can be cached, up to the cachability limit of the processor.

For information about	Refer to
Processor support for the D810E2CB board	http://support.intel.com/support/motherboards/desktop
Processor data sheets	http://www.intel.com/design/litcentr

1.5 System Memory

NOTE

To be compliant with applicable Intel® SDRAM memory specifications, the D810E2CB board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. If your memory modules do not support SPD, the BIOS will attempt to configure the memory controller for normal operation; however, the DIMMs may not function at their optimum speed.

CAUTION

Before installing or removing memory, make sure that AC power has been removed by unplugging the power cord from the computer. Failure to do so could damage the memory and the board.

CAUTION

Because the main system memory is also used as video memory, the board requires 100 MHz SDRAM DIMMs even though the processor's system bus speed is 66 MHz. It is highly recommended that SPD DIMMs be used, since this allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted.

The D810E2CB board has two DIMM sockets. The minimum memory size is 64 MB and the maximum memory size is 512 MB. The BIOS automatically detects memory type, size, and speed. Memory can be installed in one or both sockets. Memory size can vary between sockets.

The D810E2CB board supports the following memory features:

- 3.3 V, 168-pin DIMMs with gold-plated contacts
- 100 MHz SDRAM
- Serial Presence Detect (SPD) or non-SPD memory (BIOS recovery requires SPD DIMMs)
- Non-ECC (64-bit) memory
- Unbuffered single- or double-sided DIMMs

The board is designed to support DIMMs in the configurations listed in Table 5 below.

Table 5. System Memory Configuration

DIMM Size	Non-ECC Configuration
16 MB	2 Mbit x 64
32 MB	4 Mbit x 64
64 MB	8 Mbit x 64
128 MB	16 Mbit x 64
256 MB	32 Mbit x 64

For information about	Refer to
The *PC Serial Presence Detect Specification*	Table 3, page 16
Obtaining copies of PC SDRAM specifications	http://www.intel.com/design/pcisets/memory

1.6 Intel® 810E Chipset

The Intel 810E chipset consists of the following devices:

- 82810E Graphics Memory Controller Hub (GMCH) with Accelerated Hub Architecture (AHA) bus
- 82801BA I/O Controller Hub (ICH2) with AHA bus
- SST 49LF004A Firmware Hub (FWH)

The GMCH is a centralized controller for the system bus, the memory bus, the AGP bus, and the Accelerated Hub Architecture interface. The ICH2 is a centralized controller for the board's I/O paths. The FWH provides the nonvolatile storage of the BIOS. The component combination provides the chipset interfaces as shown in Figure 3.

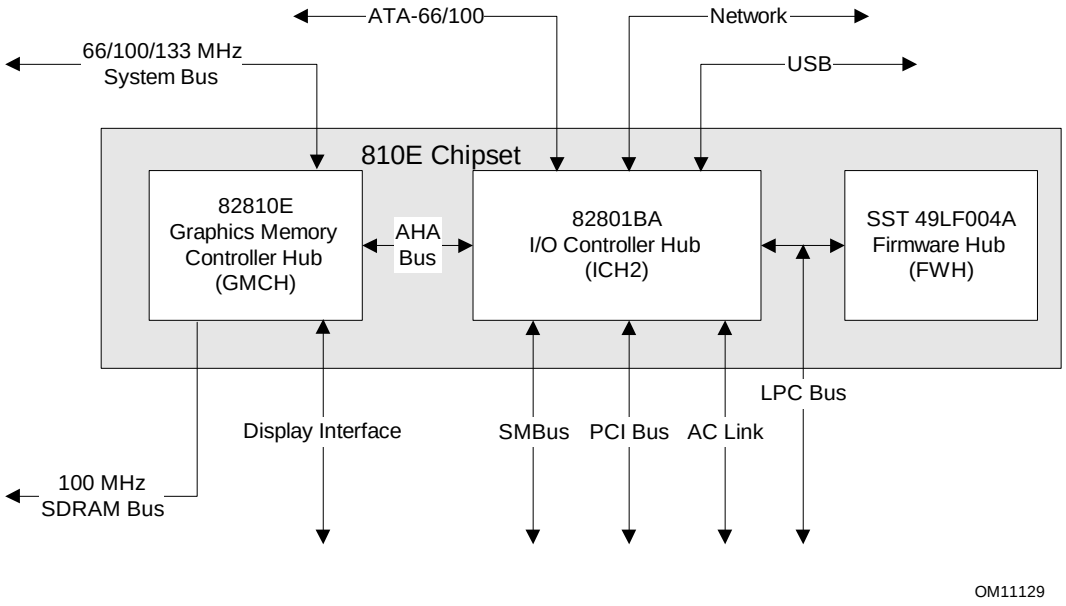


Figure 3. Intel 810E Chipset Block Diagram

For information about	Refer to
The Intel 810E chipset	http://www.developer.intel.com
The resources used by the chipset	Chapter 2
The chipset's compliance with ACPI and AC '97	Table 3, page 16

1.6.1 Direct AGP

Direct (integrated) AGP is a high-performance bus (independent of the PCI bus) for graphics-intensive applications, such as 3D applications. AGP overcomes certain limitations of the PCI bus related to handling large amount of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent bus efficiency

For information about	Refer to
The location of the VGA port connector	Figure 5, page 46
Obtaining the *Accelerated Graphics Port Interface Specification*	Table 3, page 16

1.6.2 USB

The ICH2 contains two separate USB controllers supporting four USB ports. One USB peripheral can be connected to each port. For more than four USB devices, an external hub can be connected to any of the ports. Two of the USB ports are implemented with stacked back panel connectors. The other two are accessible via the front panel USB connector at location J8B1. The D810E2CB board fully supports Universal Hub Controller Interface (UHCI) and uses UHCI-compatible software drivers.

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

For information about	Refer to
The location of the USB connectors on the back panel	Figure 5, page 46
The signal names of the USB connectors on the back panel	Table 21, page 47
The location of the USB connectors on the front panel	Figure 8, page 58
The signal names of the USB connectors on the front panel	Table 41, page 60
The USB and UHCI specifications	Table 3, page 16

1.6.3 IDE Support

The ICH2's IDE controller has two independent bus-mastering IDE interfaces that can be independently enabled. The IDE interfaces support the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- Ultra ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- Ultra ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH2 Ultra ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

NOTE

ATA-100 and ATA-66 use faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.

The IDE interfaces also support ATAPI devices (such as CD-ROM drives) and ATA devices using the transfer modes listed in Section 4.4.4.1 on page 91.

The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The D810E2CB board supports laser servo (LS-120) diskette technology through its IDE interfaces. An LS-120 drive can be configured as a boot device by setting the BIOS Setup program's Boot menu to one of the following:

- ARMD-FDD (ATAPI removable media device – floppy disk drive)
- ARMD-HDD (ATAPI removable media device – hard disk drive)

For information about	Refer to
The location of the IDE connectors	Figure 7, page 54
The signal names of the IDE connectors	Table 36, page 56
BIOS Setup program's Boot menu	Table 66, page 98

1.6.4 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multicentury calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3.3 V standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

The time, date, and CMOS values can be specified in the BIOS Setup program. The CMOS values can be returned to their defaults by using the BIOS Setup program.

NOTE

If the battery and AC power fail, the last saved defaults, custom or standard, will be loaded into CMOS SRAM at power on.

NOTE

The recommended method of accessing the date in systems with Intel® desktop boards is indirectly from the Real-Time Clock (RTC) via the BIOS. The BIOS on Intel desktop boards contains a century checking and maintenance feature. This feature checks the two least significant digits of the year stored in the RTC during each BIOS request (INT 1Ah) to read the date and, if less than 80 (i.e., 1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.

For information about	Refer to
Proper date access in systems with Intel desktop boards	http://support.intel.com/support/year2000/

1.6.5 SST 49LF004A 4 Mbit Firmware Hub (FWH)

The FWH provides the following:

- System BIOS program
- System security and manageability logic that enables protection for storing and updating of platform information

1.7 I/O Controller

The SMSC LPC47M102 I/O controller provides the following features:

- 3.3 V operation
- One serial port
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.2 MB or 1.44 MB diskette drive
- Intelligent power management, including a programmable wake up event interface
- PCI power management support

The BIOS Setup program provides configuration options for the I/O controller.

For information about	Refer to
SMSC LPC47M102 I/O controller	http://www.smsc.com

1.7.1 Serial Port

The D810E2CB board has one serial port connector on the back panel. The serial port's NS16C550-compatible UART supports data transfers at speeds up to 115.2 kbits/sec with BIOS support. The serial port can be assigned as COM1 (3F8h), COM2 (2F8h), COM3 (3E8h), or COM4 (2E8h).

For information about	Refer to
The location of the serial port connector	Figure 5, page 46
The signal names of the serial port connector	Table 24, page 48

1.7.2 Parallel Port

The connector for the multimode bidirectional parallel port is a 25-pin D-Sub connector located on the back panel. In the BIOS Setup program, the parallel port can be configured for the following:

- Output only (PC AT†-compatible mode)
- Bi-directional (PS/2 compatible)
- EPP
- ECP

For information about	Refer to
The location of the parallel port connector	Figure 5, page 46
The signal names of the parallel port connector	Table 22, page 47

1.7.3 Diskette Drive Controller

The I/O controller supports one diskette drive that is compatible with the 82077 diskette drive controller and supports both PC-AT and PS/2 modes.

For information about	Refer to
The location of the diskette drive connector	Figure 7, page 54
The signal names of the diskette drive connector	Table 37, page 57
The supported diskette drive capacities and sizes	Table 61, page 93

1.7.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the AMI keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power-on/reset. A power-on/reset password can be specified in the BIOS Setup program.

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 5, page 46
The signal names of the keyboard and mouse connectors	Table 20, page 47

1.8 Graphics Subsystem

The Intel 82810E GMCH graphics memory controller hub component provides the following graphics support features:

- Integrated 2-D and 3-D graphics engines
- Integrated hardware motion compression engine
- Integrated 230 MHz DAC

Table 6 lists the refresh rates supported by the graphics subsystem.

Table 6. Supported Graphics Refresh Rates

Resolution	Available Refresh Rates (Hz)
640 x 200 x 16 colors	70
640 x 350 x 16 colors	70
640 x 400 x 256 colors	60, 70, 75, 85
640 x 400 x 64 K colors	60, 70, 75, 85
640 x 400 x 16 M colors	70
640 x 480 x 16 colors	60, 72, 75, 85
640 x 480 x 256 colors	60, 70, 72, 75, 85
640 x 480 x 32 K colors	60, 75, 85
640 x 480 x 64 K colors	60, 70, 72, 75, 85
640 x 480 x 16 M colors	60, 70, 72, 75, 85
800 x 600 x 256 colors	60, 75, 85
800 x 600 x 32 K colors	60, 70, 72, 75, 85
800 x 600 x 64 K colors	60, 70, 72, 75, 85
800 x 600 x 16 M colors	60, 70, 72, 75, 85
1024 x 768 x 256 colors	60, 70, 75, 85
1024 x 768 x 32 K colors	60, 75, 85
1024 x 768 x 64 K colors	60, 70, 72, 75, 85
1024 x 768 x 16 M colors	60, 70, 72, 75, 85
1056 x 800 x 16 colors	70
1280 x 1024 x 256 colors	60, 70, 72, 75, 85
1280 x 1024 x 32 K colors	60, 75, 85
1280 x 1024 x 64 K colors	60, 70, 72, 75
1280 x 1024 x 16 M colors	60, 70, 72, 75, 85

For information about	Refer to
Obtaining graphics software and utilities	http://support.intel.com/support/motherboards/desktop

1.9 Audio Subsystem

The D810E2CB board includes an Audio Codec ’97 (AC ’97) compatible audio subsystem consisting of these devices:

- Intel 82801BA ICH2 (AC link output)
- CS4201 analog codec

Figure 4 is a block diagram of the audio subsystem.

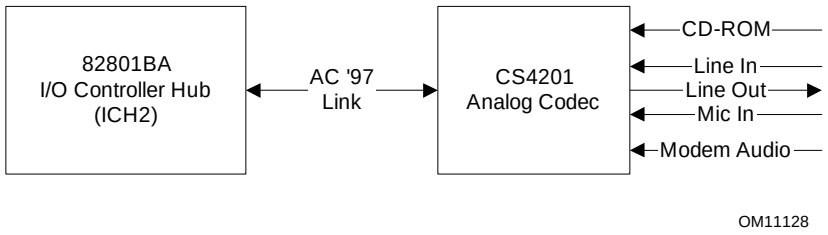


Figure 4. Block Diagram of Audio Subsystem with CS4201 Codec

Features of the audio subsystem include:

- Independent channels for PCM in, PCM out, and Mic in
- 16-bit stereo I/O up to 48 kHz
- Multiple sample rates

For information about	Refer to
Obtaining audio software and utilities	Section 1.2, page 16

1.9.1 CS4201 Analog Codec

The CS4201 is a fully AC ’97 compliant codec. The codec's features include:

- 16-bit stereo full-duplex operation
- High quality CD-ROM input with ground sense
- Stereo line level output
- Power management support
- Full duplex variable sampling rate (7 kHz to 48 kHz) with 1 Hz resolution
- Phat† Stereo 3-D stereo enhancement

1.9.2 Audio Connectors

The audio connectors include the following:

- ATAPI CD-ROM (connects an internal ATAPI CD-ROM drive to the audio mixer)
- Telephony
- Line out (back panel)
- Line in (back panel)
- Mic in

For information about	Refer to
The location of the ATAPI CD-ROM and telephony connectors	Figure 6, page 51
The signal names of the ATAPI CD-ROM connector	Table 29, page 52
The signal names of the telephony connector	Table 30, page 52
The back panel audio connectors	Section 2.8.1, page 46

1.10 Hardware Management Subsystem

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including the following:

- Fan control and monitoring
- Thermal and voltage monitoring

For information about	Refer to
The WfM specification	Table 3, page 16

1.10.1 Hardware Monitor Component (Optional)

The hardware monitor component provides low-cost instrumentation capabilities. The features of the component include:

- Internal ambient temperature sensing
- Remote thermal diode sensing for direct monitoring of processor temperature
- Power supply monitoring (+12 V, +5 V, +3.3 V, +2.5 V, 3.3 VSB, Vccp) to detect levels above or below acceptable values
- SMBus interface

The hardware monitor component enables the board to be compatible with the Wired for Management (WfM) specification.

For information about	Refer to
The board's compatibility with the WfM specification	Table 3, page 16

1.10.2 Fan Control and Monitoring

The SMSC LPC47M102 I/O controller provides two fan sense inputs and two fan control outputs. Monitoring and control can be implemented using third-party software.

For information about	Refer to
The functions of the fan connectors	Section 1.12.3.2, page 35
The locations of the fan connectors	Figure 6, page 51
The signal names of the fan connectors	Section 2.8.2.1, page 51

1.11 LAN Subsystem (Optional)

The Network Interface Controller subsystem consists of the ICH2 (with integrated LAN Media Access Controller) and a physical layer interface device. Features of the LAN subsystem include:

- PCI Bus Master interface
- CSMA/CD Protocol Engine
- Serial CSMA/CD unit interface that supports the 82562ET (10/100 Mbit/sec Ethernet) physical layer interface device
- PCI Power Management
  - — Supports APM
  - — Supports ACPI technology
  - — Supports Wake up from suspend state (Wake on LAN† technology)

For information about	Refer to
Obtaining LAN software and drivers	Section 1.2, page 16

1.11.1 Intel® 82562ET Platform LAN Connect Device

The Intel 82562ET component provides an interface to the back panel RJ-45 connector with integrated LEDs. This physical interface may alternately be provided via the CNR connector.

The Intel 82562ET provides the following functions:

- Basic 10/100 Ethernet LAN connectivity
- Supports RJ-45 connector with status indicator LEDs on the back panel
- Full device driver compatibility
- Advanced Power Management and ACPI support
- Programmable transit threshold
- Configuration EEPROM that contains the MAC address
- Remote monitoring (alerting)

1.11.2 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector. Table 7 describes the LED states when the board is powered up and the LAN subsystem is operating.

Table 7. LAN Connector LED States

LED Color	LED State	Condition
Green	Off	10 Mbit/sec data rate is selected.
	On	100 Mbit/sec data rate is selected.
Yellow	Off	LAN link is not established.
	On (steady state)	LAN link is established.
	On (brighter and pulsing)	The computer is communicating with another computer on the LAN.

1.12 Power Management Features

Power management is implemented at several levels, including:

- Advanced Configuration and Power Interface (ACPI)
- Advanced Power Management (APM)
- Hardware support:
  - Power connector
  - Fan connectors
  - Wake on LAN technology
  - Instantly Available† technology
  - Wake on Ring
  - Resume on Ring
  - Wake from USB
  - PME# wakeup support

1.12.1 ACPI

If the board is used with an ACPI-aware operating system, the BIOS can provide ACPI support. ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with this board requires the support of an operating system that provides full ACPI functionality. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, video displays, and hard disk drives
- Methods for achieving less than 30-watt system operation in the Power On Suspend sleeping state, and less than 5-watt system operation in the Suspend to RAM sleeping state
- A Soft-off feature that enables the operating system to power off the computer
- Support for multiple wake up events (see Table 10 on page 33)
- Support for a front panel power and sleep mode switch.

Table 8 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 8. Effects of Pressing the Power Switch

If the system is in this state…		…and the power switch is pressed for	…the system enters this state
Off	(ACPI G2/S5 state)	Less than four seconds	Power on
On	(ACPI G0 state)	Less than four seconds	Soft off/Suspend
On	(ACPI G0 state)	More than four seconds	Fail safe power off
Sleep	(ACPI G1 state)	Less than four seconds	Wake up
Sleep	(ACPI G1 state)	More than four seconds	Power off

For information about	Refer to
The board's compliance level with ACPI	Table 3, page 16

1.12.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 9 lists the power states supported by the board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 9. Power States and Targeted System Power

Global States	Sleeping States	CPU States	Device States	Targeted System Power*
G0 - working state	S0 - working	C0 - working	D0 - working state	Full power > 30 W
G1 - sleeping state	S1 - CPU stopped	C1 - stop grant	D1, D2, D3 - device specification specific.	5 W < power < 30 W
G1 - sleeping state	S3 - Suspend-to-RAM. Context saved to RAM.	No power	D3 - no power except for wake up logic.	Power < 5 W **
G2/S5	S5 - Soft off. Context not saved. Cold boot is required.	No power	D3 - no power except for wake up logic.	Power < 5 W **
G3 - mechanical off. (AC power is disconnected from the computer.)	No power to the system.	No power	D3 - no power for wake up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

* Total system power is dependent on the system configuration, including peripherals powered by the system chassis' power supply.

** Dependent on the standby power consumption of wake-up devices used in the system.

1.12.1.2 Wake-up Devices and Events

Table 10 lists the devices or specific events that can wake the computer from specific states.

Table 10. ACPI Wake-up Devices and Events

These devices/events can wake-up the computer…	…from this state
Power switch	S1, S3, S5
RTC alarm	S1, S3, S5
LAN	S1, S3
PME#	S1, S3
USB	S1, S3
PS/2	S1, S3

1.12.1.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure devices that do not have other hardware standards for enumeration and configuration. PCI devices on a desktop board, for example, are not enumerated by ACPI.

1.12.2 APM

APM makes it possible for the computer to enter an energy saving standby mode. The standby mode can be initiated in the following ways:

- Time-out period specified in the BIOS Setup program
- Suspend/Resume switch connected to the front panel sleep connector
- From the operating system, such as the Suspend menu item in Windows 98 SE

In standby mode, the board can reduce power consumption by spinning down hard drives, and reducing power to or turning off VESA† DPMS-compliant monitors. Power-management mode can be enabled or disabled in the BIOS Setup program.

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default, but the operating system must support an APM driver for the power-management features to work. For example, Windows 98 SE supports the power-management features upon detecting that APM is enabled in the BIOS.

Table 11 lists the devices or specific events that can wake the computer from specific states.

Table 11. APM Wake-up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	Soft-off
RTC alarm*	Soft-off, suspend
LAN	Soft-off, suspend
PME#	Soft-off, suspend
USB	Suspend
PS/2	Suspend

* Unattended Wake Mode – display will be video BIOS string only

For information about	Refer to
Enabling or disabling power management in the BIOS Setup program	Section 4.6, page 97
The board's compliance level with APM	Table 3, page 16

1.12.3 Hardware Support

CAUTION

If Wake on LAN and Instantly Available technology features are used, the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.11.2 on page 66 for additional information.

The board provides several hardware features that support power management, including:

- Power connector
- Fan connectors
- Wake on LAN technology
- Instantly Available technology
- Wake on Ring
- Resume on Ring
- Wake from USB
- PME# wakeup support

Wake on LAN technology and Instantly Available technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

Wake on Ring and Resume on Ring enable telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal) and the ACPI or APM state being used.

NOTE

The use of Wake on Ring, Resume on Ring, and Wake from USB technologies from an ACPI state require the support of an operating system that provides full ACPI functionality.

1.12.3.1 Power Connector

When used with an ATX-compliant power supply that supports remote power on/off, the D810E2CB board can turn off the system power through software control.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

For information about	Refer to
The location of the power connector	Figure 6, page 51
The signal names of the power connector	Table 32, page 53
The ATX specification	Table 3, page 16
The MicroATX specification and the SFX Power Supply Design Guide	Table 3, page 16

1.12.3.2 Fan Connectors

Table 12 describes the functions of the fan connectors.

Table 12. Fan Connector Descriptions

Connector	Function
Processor fan (fan 1)	Provides +12 V DC for a processor fan or active fan heatsink.
Chassis fan (fan 2)	Provides +12 V DC for a system or chassis fan.

For information about	Refer to
The location of the fan connectors	Figure 6, page 51
The signal names of the processor fan connector	Table 31, page 52
The signal names of the chassis fan connector	Table 34, page 53

1.12.3.3 Wake on LAN Technology

⚠ CAUTION

For Wake on LAN technology, the 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Wake on LAN technology can damage the power supply. Refer to Section 2.11.2 on page 66 for additional information.

Wake on LAN technology enables remote wakeup of the computer through a network. The LAN subsystem monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet† frame, the LAN subsystem asserts a wakeup signal that powers up the computer. The D810E2CB board supports Wake on LAN technology through the PCI bus PME# signal.

1.12.3.4 Instantly Available Technology

⚠ CAUTION

For Instantly Available technology, the 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when using this feature can damage the power supply. Refer to Section 2.11.2 on page 66 for additional information.

Instantly Available technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off. The power supply appears to be off, the fans are off, and the front panel power LED will be yellow (unless a single color LED is installed, in which case, it will be off.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 10 on page 33 lists the devices and events that can wake the computer from the S3 state.

The D810E2CB board supports the *PCI Bus Power Management Interface Specification*. For information on the versions of this specification, see Section 1.3. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available technology requires operating system support and PCI 2.2 compliant add-in cards and drivers.

1.12.3.5 Wake on Ring

⟹ NOTE

Wake on Ring requires the use of a modem (external USB, or modem connected to serial port A) that supports the Wake on Ring feature.

The operation of Wake on Ring can be summarized as follows:

- Powers up the computer from the ACPI S5 state or from APM soft-off mode
- Requires two calls to access the computer:
  - — First call restores the computer from an ACPI S5 state or powers up the computer from APM soft-off mode.
  - — Second call enables access (when the appropriate software is loaded).
- Detects incoming calls for external USB modems. The USB bus is monitored for the RING_DETECT signal.

Table 13 outlines wake on ring support for modems.

Table 13. Wake on Ring Support for Modems

State	USB Modem	Serial Port Modem	PCI Bus Modem (via PME#)
S1	Refer to Section 1.12.3.6	Refer to Section 1.12.3.6	Supported
S3	Supported	Supported	Supported
S5	Not supported	Supported	Not supported
Soft-off	Not supported	Supported	Supported
Suspend	Refer to Section 1.12.3.6	Refer to Section 1.12.3.6	Supported

1.12.3.6 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from the ACPI S1 state or APM suspend mode
- Requires only one call to access the computer
- Detects incoming call similarly for external and internal modems

1.12.3.7 Wake from USB

USB bus activity wakes the computer from an ACPI S1 or S3 state or APM suspend mode.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB. Wake from USB is not supported in APM soft-off mode.

1.12.3.8 PME# Wakeup Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1 or S3 state.

2 Technical Reference

What This Chapter Contains

2.1 Introduction

Sections 2.2 – 2.6 contain several standalone tables. Table 14 describes the system memory map, Table 15 shows the I/O map, Table 16 lists the DMA channels, Table 17 defines the PCI configuration space map, and Table 18 describes the interrupts. The remaining sections in this chapter are introduced by text found with their respective section headings.

2.2 Memory Map

Table 14. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 524288 K	100000 - 1FFFFFFF	511 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to PCI bus)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.3 I/O Map

Table 15. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	DMA controller
0020 - 0021	2 bytes	Programmable Interrupt Controller (PIC)
0040 - 0043	4 bytes	System timer
0060	1 byte	Keyboard controller byte – reset IRQ
0061	1 byte	System speaker
0064	1 byte	Keyboard controller, CMD/STAT byte
0070 - 0071	2 bytes	System CMOS / Real-Time Clock (RTC)
0072 - 0073	2 bytes	System CMOS
0080 - 008F	16 bytes	DMA controller
0092	1 byte	Fast A20 and PIC
00A0 - 00A1	2 bytes	PIC
00B2 - 00B3	2 bytes	Reserved
00C0 - 00DF	32 bytes	DMA
00F0	1 byte	Numeric data processor
0170 - 0177	8 bytes	Secondary IDE channel
01F0 - 01F7	8 bytes	Primary IDE channel
02E8 - 02EF[1]	8 bytes	COM4/video (8514A)
02F8 - 02FF[1]	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0377, bits 6:0	7 bits	Secondary IDE channel status port
03B0 - 03BB	12 bytes	Intel 82810E – DC100 Graphics/Memory Controller Hub (GMCH)
03C0 - 03DF	32 byte	Intel 82810E – Graphics/Memory Controller Hub (GMCH)
03E8 - 03EF	8 bytes	COM3
03F6	1 byte	Primary IDE channel command port
03F8 - 03FF	8 bytes	COM1

continued

Table 15. I/O Map (continued)

Address (hex)	Size	Description
04D0 - 04D1	2 bytes	Edge/level triggered PIC
0CF8 - 0CFB[2]	4 bytes	PCI configuration address register
0CF9[3]	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
E800 - E8FF	256 bytes	ICH2 Audio controller
EF00 - EF3F	64 bytes	ICH2 Audio bus master
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers
96 contiguous bytes starting on a 128-byte divisible boundary		ICH2 (ACPI + TCO)
64 contiguous bytes starting on a 64-byte divisible boundary		D810E2CB Board Resource
64 contiguous bytes starting on a 64-byte divisible boundary		ICH2 LAN controller
32 contiguous bytes starting on a 32-byte divisible boundary		ICH2 (USB Controller #1)
32 contiguous bytes starting on a 32-byte divisible boundary		ICH2 (USB Controller #2)
16 contiguous bytes starting on a 16-byte divisible boundary		ICH2 (SMBus)
4096 contiguous bytes starting on a 4096-byte divisible boundary		Intel 82801BA PCI Bridge
96 contiguous bytes starting on a 128-byte divisible boundary		LPC47M102 I/O controller

Notes:

1. Default, but can be changed to another address range
2. Dword access only
3. Byte access only

NOTE

Some additional I/O addresses are not available due to ICH2 addresses aliasing.

For information about	Refer to
ICH2 addressing	Section 1.2, page 16

2.4 DMA Channels

Table 16. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8- or 16-bits	Open
1	8- or 16-bits	Open
2	8- or 16-bits	Open
3	8- or 16-bits	Open / ECP
4		Reserved - cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

2.5 PCI Configuration Space Map

Table 17. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82810E component
00	01	00	Graphics controller of Intel 82810E component
00	1E	00	Link to PCI bridge
00	1F	00	PCI-to-LPC bridge
00	1F	01	IDE controller
00	1F	02	USB controller #1
00	1F	03	SMBus controller
00	1F	04	USB controller #2
00	1F	05	AC '97 audio controller
00	1F	06	AC '97 modem controller
01	08	00	ICH2 LAN controller (optional)
01	09	00	PCI bus connector 1 (J3B1)
01	0A	00	PCI bus connector 2 (J3A2)

2.6 Interrupts

Table 18. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2*
4	COM1*
5	LAN / User available
6	User available
7	LPT1 (Parallel port if present, or else, user available) / ECP
8	Real-time clock
9	Reserved for ICH2 system management bus / Audio
10	User available
11	User available
12	Onboard mouse port (if present, or else, user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, or else, user available)
15	Secondary IDE (if present, or else, user available)

* Default, but can be changed to another IRQ

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the onboard PCI devices. The PCI specification shows how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices.

The ICH2 PCI-to-LPC bridge has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources connect to one of these PIRQ signals. Because there are only eight signals, some PCI interrupt sources are mechanically tied together on the D810E2CB board and therefore share the same interrupt.

Table 19 lists the PIRQ signals and shows how the signals are connected to the onboard PCI interrupt sources.

For example, using as a reference, assume an add-in card using INTA is plugged into PCI bus connector 2. In PCI bus connector 2, INTA is connected to PIRQF, which is already connected to the SMBus. The add-in card in PCI bus connector 2 now shares interrupts with these onboard interrupt sources.

Table 19. PCI Interrupt Routing Map

PCI Interrupt Source	ICH2 PIRQ Signal Name				
	PIRQC	**PIRQF**	**PIRQG**	**PIRQB**	**Other**
ICH2 USB controller					INTD to PIRQD
SMBus controller				INTB	
ICH2 USB controller					INTC to PIRQH
ICH2 Audio				INTB	
ICH2 LAN					INTA to PIRQE
PCI Bus Connector 1 (J3B1)	INTA	INTB	INTC	INTD	
PCI Bus Connector 2 (J3A2)	INTD	INTA	INTB	INTC	

NOTE

The ICH2 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 10, 11, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

2.8 Connectors

CAUTION

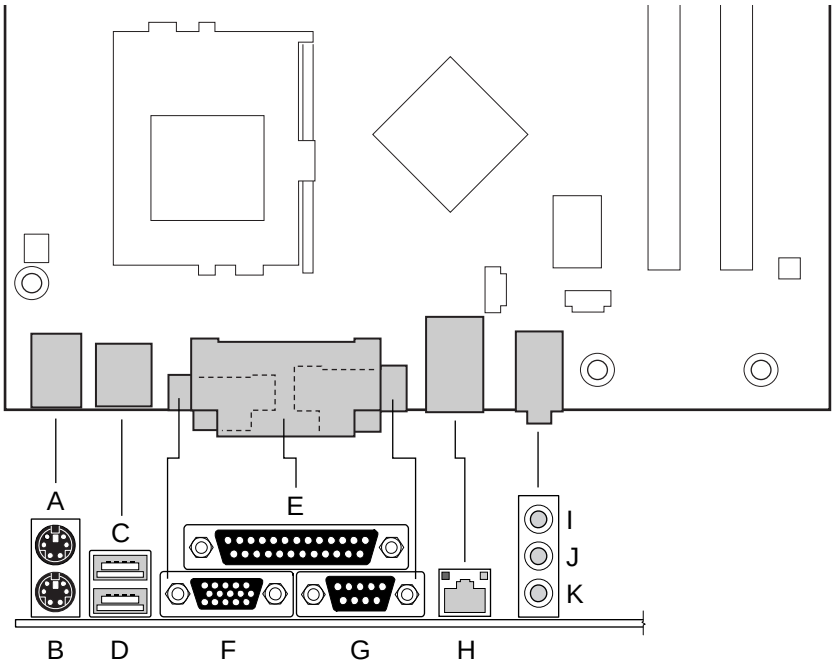
Only the back panel connectors of the board and the front panel USB connectors have overcurrent protection. The other internal board connectors are not overcurrent protected and should connect only to devices inside the computer chassis such as fans and internal peripherals. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by an external device may result in a high output current that could damage the D810E2CB board, the interconnecting cable, and the external device itself.

This section describes the D810E2CB board's connectors. The connectors can be divided into the following three groups:

- Back panel I/O connectors (see page 46)
  - PS/2 keyboard and mouse
  - USB (two)
  - Parallel port
  - VGA
  - Serial port
  - LAN
  - Audio (Line out, Line in, and Mic in)
- Internal I/O connectors (see page 50)
  - Audio (ATAPI CD-ROM and telephony)
  - Fans (2)
  - Power
  - Chassis intrusion
  - Add-in boards (two PCI bus connectors)
  - IDE (two)
  - Diskette drive
- External I/O connectors (see page 58)
  - Front panel (power/sleep/message-waiting LED, power switch, hard drive activity LED, reset switch, and infrared port)
  - Front panel USB

2.8.1 Back Panel Connectors

Figure 5 shows the location of the back panel connectors.



Item	Description	Connector Color	For additional Information…
A	PS/2 mouse port	Lime green	See Table 20, page 47
B	PS/2 keyboard port	Purple	See Table 20, page 47
C	USB port 0	Black	See Table 21, page 47
D	USB port 1	Black	See Table 21, page 47
E	Parallel port	Burgundy	See Table 22, page 47
F	VGA	Blue	See Table 23, page 48
G	Serial port A	Teal	See Table 24, page 48
H	LAN (optional)	Not color specific	See Table 25, page 48
I	Audio Line In	Light blue	See Table 26, page 49
J	Audio Line Out	Lime green	See Table 27, page 49
K	Mic In	Pink	See Table 28, page 49

Figure 5. Back Panel Connectors

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality may occur if passive (non-amplified) speakers are connected to this output.

Table 20. PS/2 Mouse/Keyboard

Pin	Signal Name
1	Data
2	Not connected
3	Ground
4	Fused +5 V
5	Clock
6	Not connected

Table 21. USB Ports 0 and 1

Pin	Signal Name
1	+5 V (fused)
2	USBP0# / USBP1#
3	USBP0 / USBP1
4	Ground

Table 22. Parallel Port

Pin	Standard Signal Name	ECP Signal Name	EPP Signal Name
1	STROBE#	STROBE#	WRITE#
2	PD0	PD0	PD0
3	PD1	PD1	PD1
4	PD2	PD2	PD2
5	PD3	PD3	PD3
6	PD4	PD4	PD4
7	PD5	PD5	PD5
8	PD6	PD6	PD6
9	PD7	PD7	PD7
10	ACK#	ACK#	INTR
11	BUSY	BUSY#, PERIPHACK	WAIT#
12	PERROR	PE, ACKREVERSE#	PE
13	SELECT	SELECT	SELECT
14	AUDOFD#	AUDOFD#, HOSTACK	DATASTB#
15	FAULT#	FAULT#, PERIPHREQST#	FAULT#
16	INIT#	INIT#, REVERSERQST#	RESET#
17	SLCTIN#	SLCTIN#	ADDRSTB#
18 – 25	GND	GND	GND

Table 23. VGA Port

Pin	Signal Name
1	Red
2	Green
3	Blue
4	No connect
5	Ground
6	Ground
7	Ground
8	Ground
9	Fused VCC
10	Ground
11	No connect
12	MONID1
13	HSYNC
14	VSYNC
15	MONID2

Table 24. Serial Port A

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	SIN# (Serial Data In)
3	SOUT# (Serial Data Out)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)

Table 25. LAN (Optional)

Pin	Signal Name
1	TX+
2	TX-
3	RX+
4	Ground
5	Ground
6	RX-
7	Ground
8	Ground

Table 26. Audio Line In

Pin	Signal Name
Tip	Audio left in
Ring	Audio right in
Sleeve	Ground

Table 27. Audio Line Out

Pin	Signal Name
Tip	Audio left out
Ring	Audio right out
Sleeve	Ground

Table 28. Mic In Connector

Pin	Signal Name
Tip	Mono in
Ring	Mic bias voltage

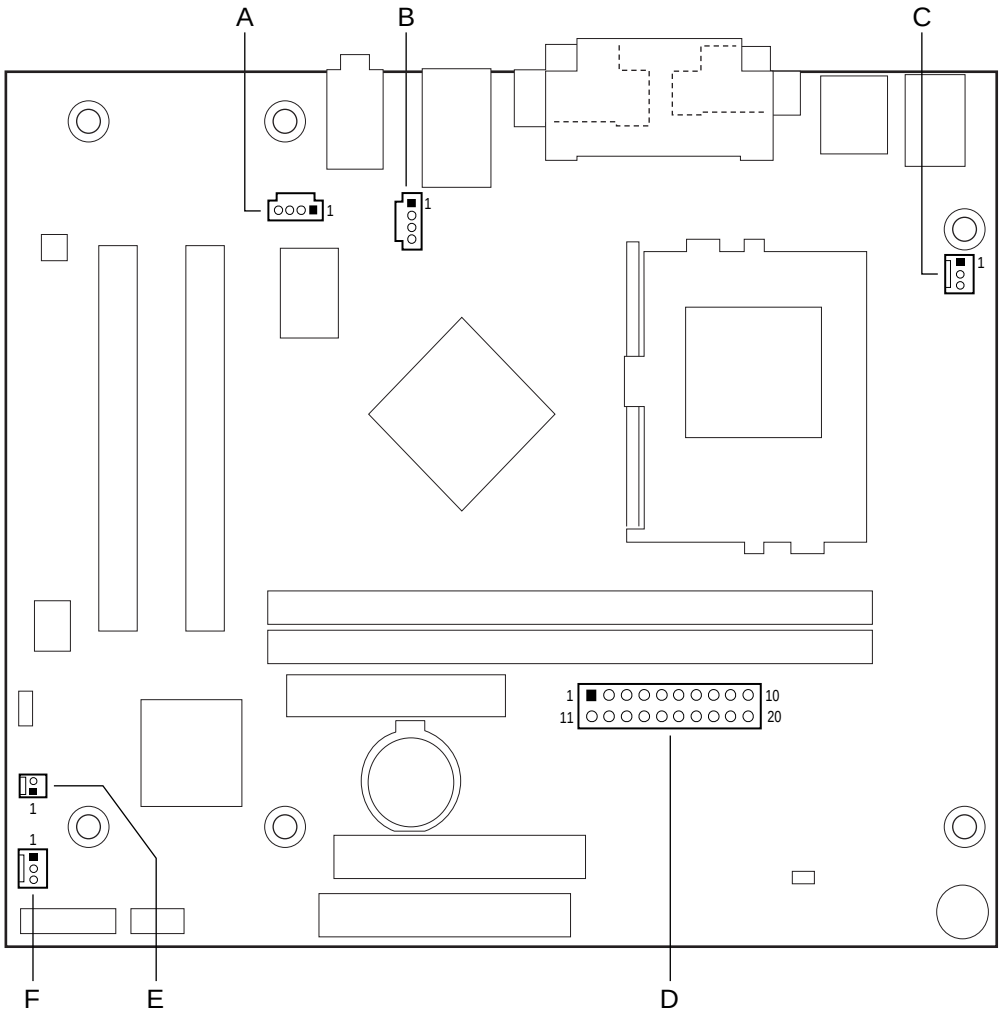
2.8.2 Internal I/O Connectors

The internal I/O connectors are divided into the following functional groups:

- Audio, power, and hardware control (see page 51)
  - ATAPI CD-ROM
  - Telephony
  - Fans (2)
  - Power
  - Chassis intrusion
- Add-in boards and peripheral interfaces (see page 54)
  - PCI bus (2)
  - IDE (2)
  - Diskette drive

2.8.2.1 Audio, Power, and Hardware Control Connectors

Figure 6 shows the location of the audio, power, and hardware control connectors.



Item	Description	Reference Designator	For additional information see…
A	ATAPI CD-ROM	J1C1 (Black)	Table 29, page 52
B	Telephony, ATAPI-style	J2D1 (Green)	Table 30, page 52
C	Processor fan (Fan 1)	J2J1	Table 31, page 52
D	Power	J6F1	Table 32, page 53
E	Chassis intrusion	J6A2	Table 33, page 53
F	Chassis fan (Fan 2)	J7A1	Table 34, page 53

Figure 6. Audio, Power, and Hardware Control Connectors

For information about…	Refer to…
The power connector	Section 1.12.3.1, page 35
The functions of the fan connectors	Section 1.12.3.2, page 35

Table 29. ATAPI CD-ROM Connector (J1C1)

Pin	Signal Name
1	Left audio input from CD-ROM
2	CD audio differential ground
3	CD audio differential ground
4	Right audio input from CD-ROM

Table 30. Telephony Connector (J2D1)

Pin	Signal Name
1	Analog audio mono input
2	Ground
3	Ground
4	Analog audio mono output

Table 31. Processor Fan Connector (J2J1)

Pin	Signal Name
1	FAN1_PWM
2	+12 V
3	FAN1_TACH

Table 32. Power Connector (J6F1)

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	Reserved
9	+5 VSB	19	+5 V
10	+12 V	20	+5 V

Table 33. Chassis Intrusion Connector (J6A2)

Pin	Signal Name
1	Intruder#
2	Ground

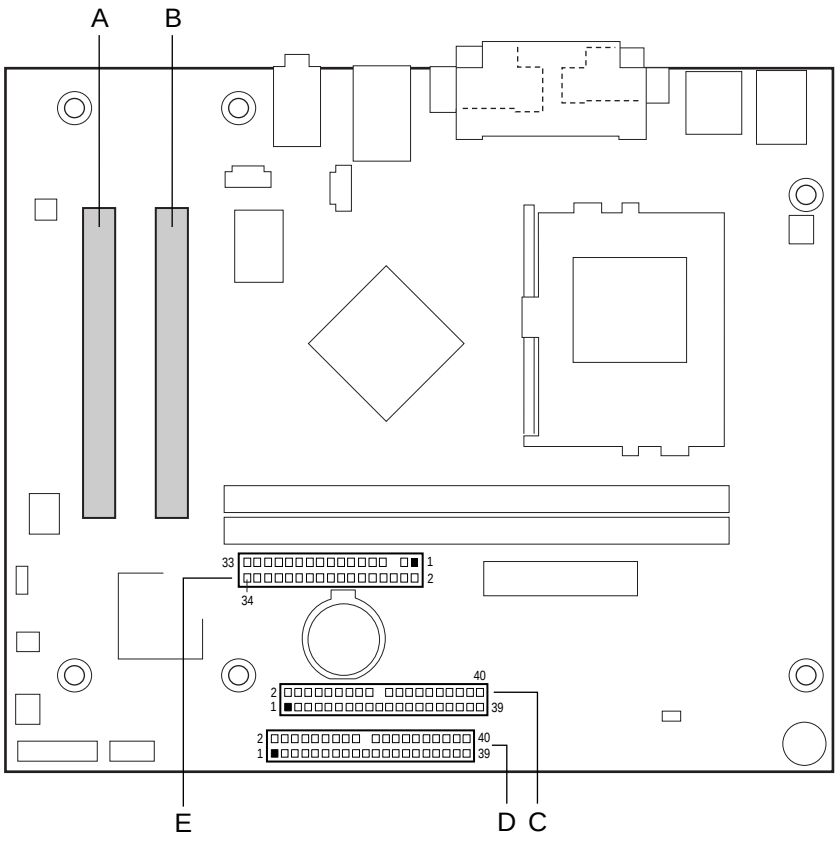
Table 34. Chassis Fan Connector (J7A1)

Pin	Signal Name
1	FAN2_PWM
2	+12 V
3	FAN2_TACH

2.8.2.2 Add-in Board and Peripheral Interface Connectors

Figure 6 shows the location of the add-in board and peripheral interface connectors. Note the following considerations for the PCI bus connectors:

- All of the PCI bus connectors are bus master capable.
- PCI bus connector 2 has SMBus signals routed to it. This enables PCI bus add-in boards with SMBus support to access sensor data on the board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40
  - The SMBus data line is connected to pin A41



Item	Description	Reference Designator	For additional information see…
A	PCI bus connector 2	J3A2	Table 35, page 55
B	PCI bus connector 1	J3B1	Table 35, page 55
C	Secondary IDE	J7E1	Table 36, page 56
D	Primary IDE	J8D1	Table 36, page 56
E	Diskette drive	J6D1	Table 37, page 57

Figure 7. Add-in Board and Peripheral Interface Connectors

Table 35. PCI Bus Connectors (J3A2 and J3B1)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground (TRST#)*	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK)*	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS)*	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI)*	B4	no connect (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	no connect (PRSNT1#)*	A40	Reserved **	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	Reserved ***	B41	+3.3 V
A11	Reserved	B11	no connect (PRSNT2#)*	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V aux	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

* These signals (in parentheses) are optional in the PCI specification and are not currently implemented.

** On PCI bus connector 2 (J3A2), this pin is connected to the SMBus clock line.

*** On PCI bus connector 2 (J3A2), this pin is connected to the SMBus data line.

Table 36. PCI IDE Connectors (J8D1, Primary and J7E1, Secondary)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	Ground
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	DAG1 (Address 1)	34	GPIO_DMA66_Detect_Pri (GPIO_DMA66_Detect_Sec)
35	DAG0 (Address 0)	36	DAG2 (Address 2)
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

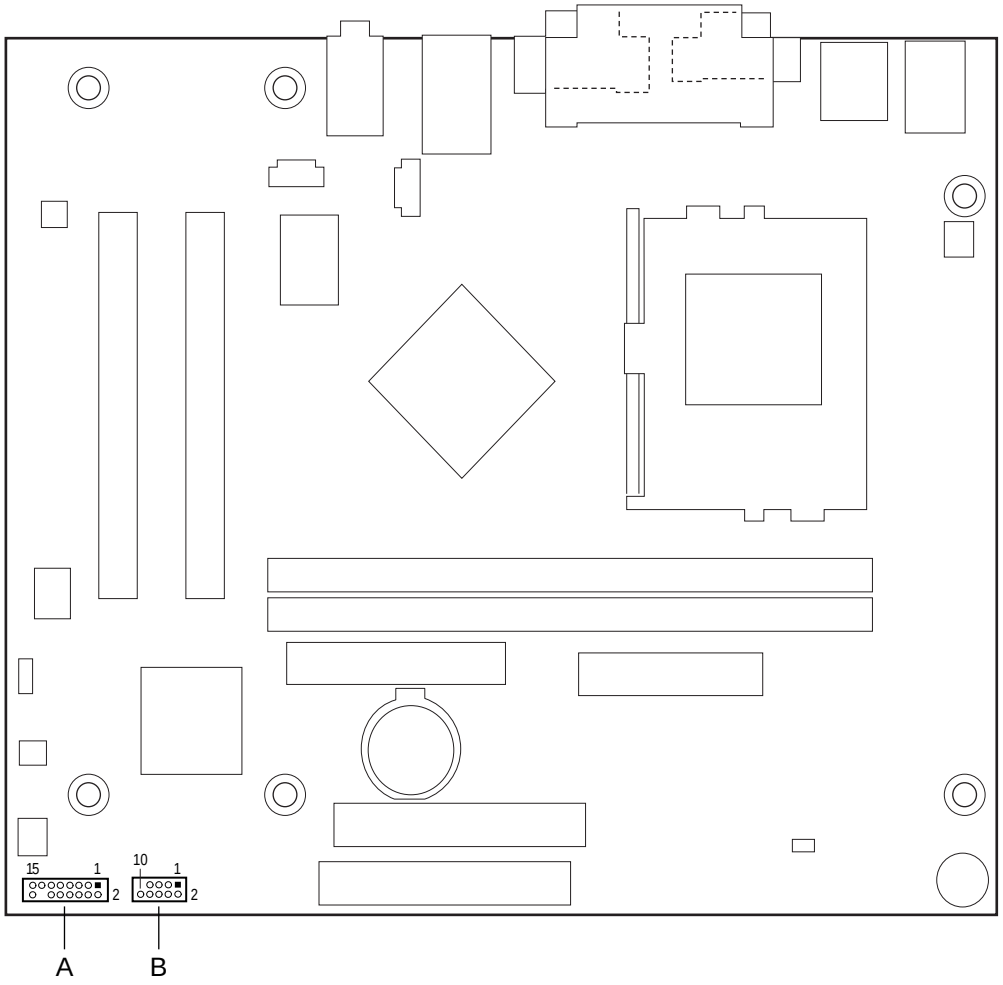
Note: Signal names in brackets ([ ]) are for the secondary IDE connector.

Table 37. Diskette Drive Connector (J6D1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	No connect
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	No connect
17	No connect	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	No connect	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

2.8.3 External I/O Connectors

Figure 8 shows the locations of the external I/O connectors.



Item	Description	Reference Designator	For more information see:
A	Front panel	J8A1	Table 38
B	Front panel USB	J8B1	Table 41

Figure 8. External I/O Connectors

2.8.3.1 Front Panel Connector

This section describes the functions of the front panel connector. Table 38 lists the signal names of the front panel connector.

Table 38. Front Panel Connector (J8A1)

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
1	HD_PWR	Out	Hard disk LED pull-up (330 Ω) to +5 V	2	HDR_BLNK_GRN	Out	Front panel green LED
3	HAD#	Out	Hard disk active LED	4	HDR_BLNK_YEL	Out	Front panel yellow LED
5	GND		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	GND		Ground
9	+5 V	Out	Power	10	N/C		
11	Reserved		Reserved	12	GND		Ground
13	GND		Ground	14	(pin removed)		Not connected
15	Reserved		Reserved	16	+5 V	Out	Power

2.8.3.1.1 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard IDE interface.

2.8.3.1.2 Power/Sleep/Message Waiting LED Connector

Pins 2 and 4 can be connected to a single- or dual-colored LED. Table 39 shows the possible states for a single-colored LED. Table 40 shows the possible states for a dual-colored LED.

Table 39. States for a One Color Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running
Blinking Green	Running/message waiting

Table 40. States for a Two Color Power LED

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting
Steady Yellow	Sleeping
Blinking Yellow	Sleeping/message waiting

NOTE

To use the message waiting function, ACPI must be enabled in the operating system and a message-capturing application must be invoked.

2.8.3.1.3 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the board resets and runs the POST.

2.8.3.1.4 Power Switch Connector

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.8.3.2 Front Panel USB Connector

Table lists the signal names of the front panel USB connector.

Table 41. Front Panel USB Connector (J8B1)

Pin	Signal Name	Pin	Signal Name
1	VREG_FP_USB_PWR	2	VREG_FP_USB_PWR
3	ICH_U_P2#	4	ICH_U_P3#
5	ICH_U_P2	6	ICH_U_P3
7	Ground	8	Ground
9	Key (no pin)	10	ICU_U_OC1_2#

2.9 Jumper Block

CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, damage to the D810E2CB board could occur.

Figure 9 shows the location of the BIOS Setup jumper block. This 3-pin jumper block determines the BIOS Setup program's mode. Table 42 describes the jumper settings for the three modes: normal, configure, and recovery.

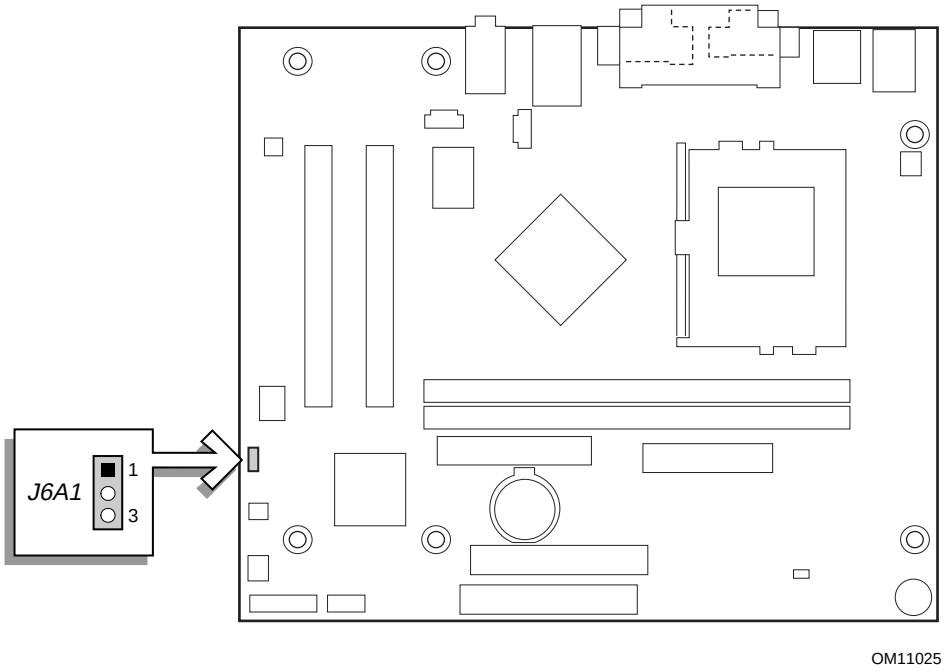
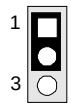
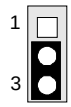
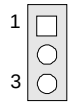


Figure 9. Location of the BIOS Setup Jumper Block

Table 42. BIOS Setup Configuration Jumper Settings (J4A1)

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None		The BIOS attempts to recover the BIOS configuration. A recovery diskette (1.44 MB) or CD–ROM is required.

For information about	Refer to
How to access the BIOS Setup program	Section 4.1, page 81
The maintenance menu of the BIOS Setup program	Section 4.2, page 82
BIOS recovery	Section 3.7, page 77

2.10 Mechanical Considerations

2.10.1 FlexATX Form Factor

The D810E2CB board is designed to fit into an ATX- or microATX-form-factor chassis. Figure 10 illustrates the mechanical form factor for the board. Dimensions are given in inches (millimeters). The outer dimensions are 9.00 inches by 7.50 inches (228.60 millimeters by 190.50 millimeters). Location of the I/O connectors and mounting holes are in compliance with the FlexATX addendum to the microATX specification (see Section 1.3).

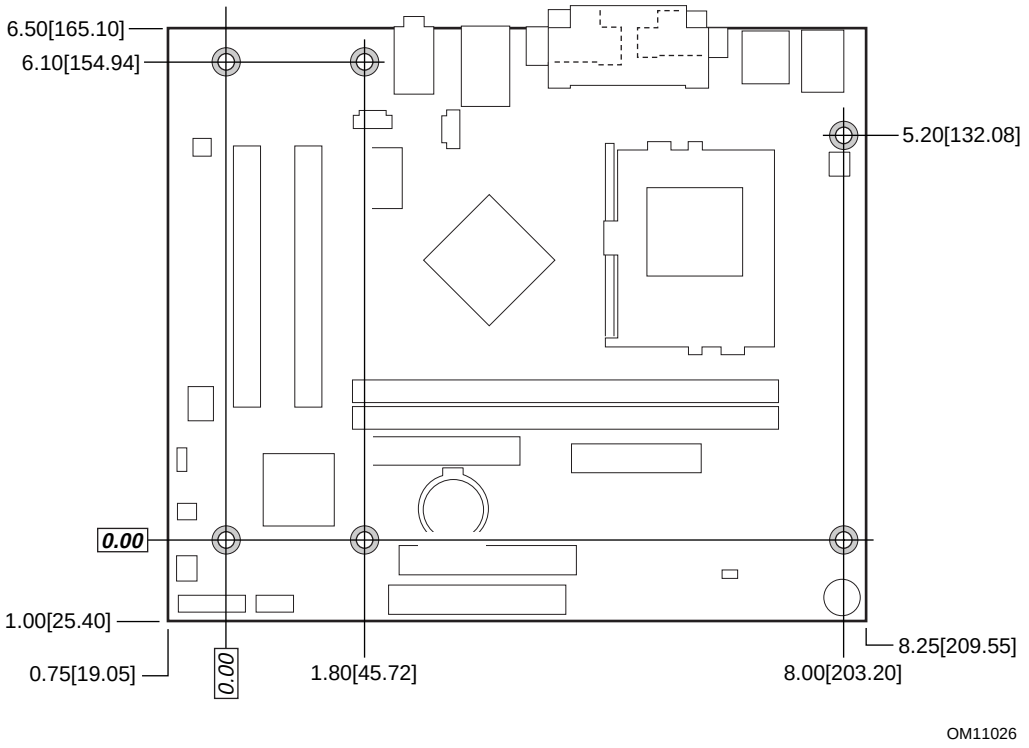


Figure 10. Board Dimensions

2.10.2 I/O Shield

The back panel I/O shield for the D810E2CB board must meet specific dimensional requirements. Systems based on this board need the back panel I/O shield to pass emissions (EMI) certification testing. Figure 11 shows the critical dimensions of the I/O shield. Dimensions are given in inches and millimeters, to a tolerance of ±0.02 inches (±5.09 millimeters). The figure indicates the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification. See Section 1.3 for information about the ATX specification.

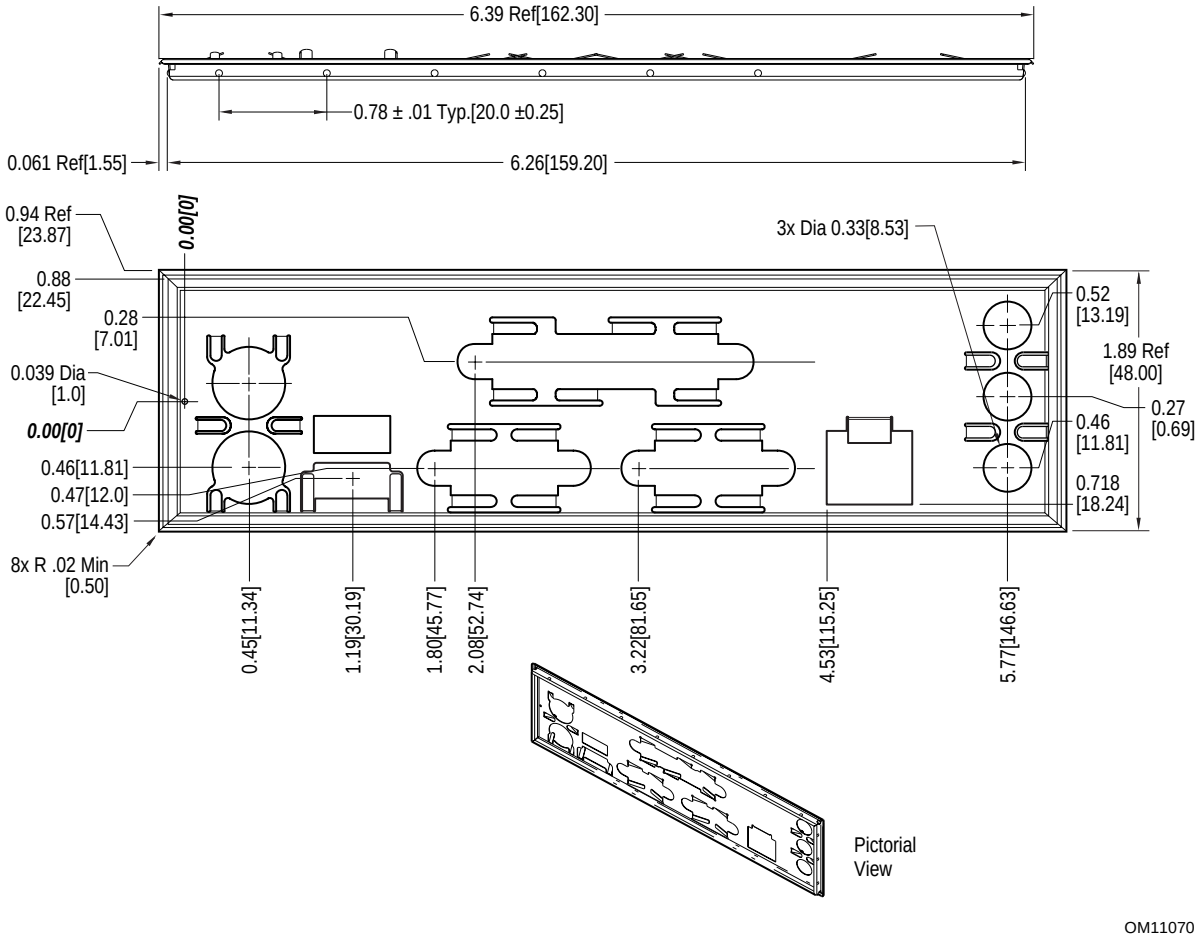


Figure 11. I/O Shield Dimensions

2.11 Electrical Considerations

2.11.1 Power Consumption

Table 43 lists voltage and current specifications for a computer that contains the D810E2CB board and the following:

- 1 GHz Intel Pentium III processor with a 256 KB cache
- 512 MB SDRAM
- 8 GB IDE hard disk drive
- 6X IDE CD-ROM drive

This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows† 98 desktop mode are measured at 640 x 480 x 256 colors and 60 Hz refresh rate. AC watts are measured with a typical 235 W power supply, nominal input voltage and frequency, with true RMS wattmeter at the line input.

Table 43. Power Usage

		DC Current at:				
Mode	**AC Power**	**+3.3 V**	**+5 V**	**+12 V**	**-12 V**	**+5 VSB**
Windows 98 ACPI S0	90 W	2.5 A	5.5 A	0.29 A	0.08 A	0.25 A
Windows 98 ACPI S1	33 W	1.72 A	0.6 A	0.2 A	0.01 A	0.245 A
Windows 98 ACPI S3	4 W	0 A	0 A	0 A	0 A	0.31 A
Windows 98 ACPI S5	3 W	0 A	0 A	0 A	0 A	0.25 A
Windows 98 SE APM On	92 W	2.4 A	5.3 A	0.29 A	0.08 A	0.25 A
Windows 98 SE APM (Note)	32 W	1.7 A	0.6 A	0.2 A	0.01 A	0.24 A

Note: Start menu/Standby

2.11.2 Power Supply Considerations

System integrators should refer to the power usage values listed in when selecting a power supply for use with this motherboard. The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification (see Section 1.3).

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

2.11.3 Standby Current Requirements

The +5 V standby current consumed by the D810E2CB desktop board is TBD. This does not include external peripherals.

NOTE

These standby current requirements are system configuration dependent.

2.11.4 Fan Power Requirements

Table 44 lists the maximum DC voltage and current requirements for the fans when the board is in sleep mode or normal operating mode. Power consumption is independent of the operating system used and other variables.

Table 44. Fan DC Power Requirements

Fan Type	Mode	Voltage	Maximum Current (Amps)
Chassis (J7A1)	Sleep	0 VDC	0 mA (current limited)
	Normal	+ 12 VDC	0.17 mA (current limited)
Processor (J2J1)	Sleep	0 VDC	0 mA (current limited)
	Normal	+ 12 VDC	0.17 mA (current limited)

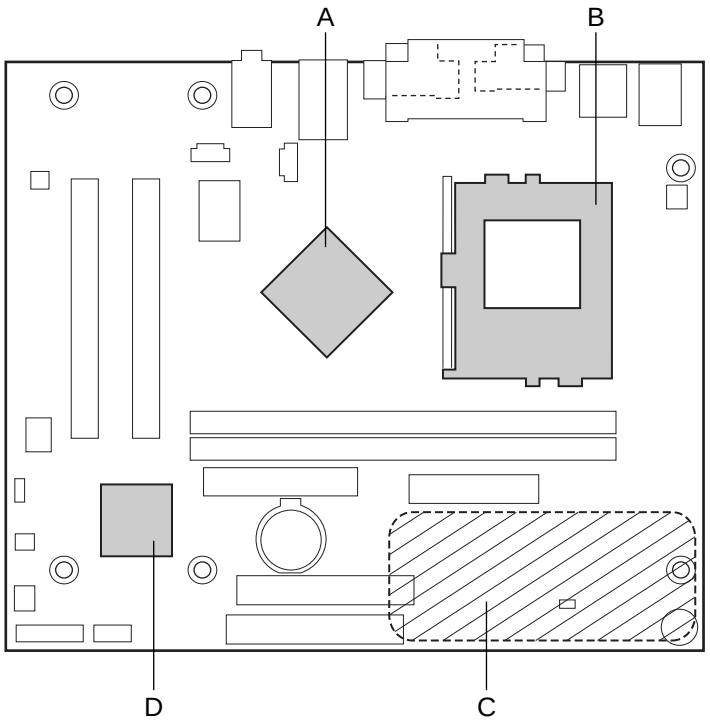
For information about	Refer to
The location of the fan connectors	Figure 6, page 51
The signal names of the processor fan connector	Table 31, page 52
The signal names of the chassis fan connector	Table 34, page 53

2.12 Thermal Considerations

CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 5 ºC to 10 ºC could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.

Figure 12 shows the localized high-temperature zones.



Item	Description
A	Intel 82810E GMCH
B	Processor
C	Processor voltage regulator area
D	Intel 82801BA ICH2

Figure 12. High Temperature Zones

Table 45 provides maximum component case temperatures for D810E2CB board components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the D810E2CB board.

Table 45. Thermal Considerations for Components

Component	Maximum Case Temperature
Intel Pentium III processor	For processor case temperature, see processor datasheets and processor specification updates
Intel Celeron processor	
Intel 82810E GMCH	70 °C (under bias)
Intel 82801BA ICH2	109 °C (under bias)

⚠ **CAUTION**

The voltage regulator area can reach a temperature of up to 85 ºC in an open chassis. Ensure that there is proper airflow to this area of the board. Failure to do so may result in damage to the voltage regulator circuit. System integrators should ensure that proper airflow is maintained in the voltage regulator circuit (item C in Figure 12). Components in this area could be damaged without adequate airflow.

2.13 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The Mean Time Between Failures (MTBF) data is calculated from predicted data at 55 ºC.

D810E2CB board MTBF: 180193.17 hours

2.14 Environmental

Table 46 lists the environmental specifications for the D810E2CB board.

Table 46. Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	30 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz: 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz: 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

2.15 Regulatory Compliance

This section describes the D810E2CB board's compliance with U.S. and international safety and electromagnetic compatibility (EMC) regulations.

2.15.1 Safety Regulations

Table 47 lists the safety regulations the D810E2CB board complies with when correctly installed in a compatible host system.

Table 47. Safety Regulations

Regulation	Title
UL 1950/CSA C22.2 No. 950, 3rd edition	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)
IEC 60950, 2nd Edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland)

2.15.2 EMC Regulations

Table 48 lists the EMC regulations the D810E2CB board complies with when correctly installed in a compatible host system.

Table 48. EMC Regulations

Regulation	Title
FCC (Class B)	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, Radiofrequency Devices. (USA)
ICES-003 (Class B)	Interference-Causing Equipment Standard, Digital Apparatus (Canada)
EN55022: 1994 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024: 1998	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
AS/NZS 3548 (Class B)	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22, 2nd Edition (Class B)	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24: 1997	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurements. (International)

2.15.3 Product Certification Markings (Board Level)

The D810E2CB desktop board has the following product certification markings:

- UL joint US/Canada Recognized Component mark: Consists of small c followed by a stylized backward UR and followed by a small US. Includes adjacent UL file number for Intel desktop boards: E210882 (component side).
- FCC Declaration of Conformity logo mark for Class B equipment; to include Intel name and D810E2CB model designation (solder side).
- CE mark: Declaring compliance to European Union (EU) EMC directive (89/336/EEC) and Low Voltage directive (73/23/EEC) (component side). The CE mark should also be on the shipping container.
- Australian Communications Authority (ACA) C-Tick mark: consists of a stylized C overlaid with a check (tick) mark (component side), followed by Intel supplier code number, N-232. The C-tick mark should also be on the shipping container.
- Printed wiring board manufacturer's recognition mark: consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0) (solder side).
- PB part number: Intel bare circuit board part number (solder side) A37815-001. Also includes SKU number starting with AA followed by additional alphanumeric characters.
- Battery "+ Side Up" marking: located on the component side of the board in close proximity to the battery holder.

3 Overview of BIOS Features

What This Chapter Contains

3.1 Introduction

The D810E2CB board uses an Intel/AMI BIOS, which is stored in flash memory and can be upgraded. In addition to the BIOS, the flash memory contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

This D810E2CB board supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as CB81010A.86A.

For information about	Refer to
The board's compliance level with Plug and Play	Table 3, page 16

3.2 BIOS Flash Memory Organization

The SST 49LF004A Firmware Hub (FWH) includes a 4 Mbit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable.

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card. Autoconfiguration information is stored in ESCD format.

For information about the versions of PCI and Plug and Play supported by the BIOS, see Section 1.3.

3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to Ultra ATA-100 and recognizes any ATAPI compliant devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 1.3 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use Ultra ATA-66/100 features the following items are required:

- An Ultra ATA-66/100 peripheral device
- An Ultra ATA-66/100 compatible cable
- Ultra ATA-66/100 operating system device drivers

NOTE

Ultra ATA-66/100 compatible cables are backward compatible with drives using slower IDE transfer protocols. If an Ultra ATA-66/100 disk drive and a disk drive using any other IDE transfer protocol are attached to the same cable, the maximum transfer rate between the drives is reduced to that of the slowest device.

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as Intel® LANDesk® Client Manager to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT† 4.0, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

For information about	Refer to
The board's compliance level with SMBIOS	Table 3, page 16

3.5 USB Legacy Support

USB legacy support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. USB legacy support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, USB legacy support is set to Enabled.

USB legacy support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. USB legacy support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if USB legacy support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and USB legacy support from the BIOS is no longer used.

To install an operating system that supports USB, verify that USB Legacy support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

NOTE

USB legacy support is for keyboards, mice, and hubs only. Other USB devices are not supported in legacy mode.

3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette (from a legacy diskette drive or an LS-120 diskette drive) or a CD-ROM.

Both utilities support the following BIOS maintenance functions:

- Verifying that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.
- Updating both the BIOS boot block and the main BIOS. This process is fault tolerant to prevent boot block corruption.
- Updating the BIOS boot block separately.
- Changing the language section of the BIOS.
- Updating replaceable BIOS modules, such as the video BIOS module.
- Inserting a custom splash screen.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 16

3.6.1 Language Support

The BIOS Setup program and help messages are supported in five languages: US English, German, Italian, French, and Spanish. The default language is US English, which is present unless another language is selected in the BIOS Setup program.

3.6.2 Custom Splash Screen

During POST, an Intel splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS upgrade utility. Information about this capability is available on the Intel Support World Wide Web site.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 16

3.7 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from either a 1.44 MB diskette (for recovery from an LS-120 diskette drive configured as an ATAPI removable IDE device), or from a CD-ROM using the BIOS recovery mode. When recovering the BIOS be aware of the following:

- Because of the small amount of code available in the nonerasable boot block area, there is no video support. You can monitor this procedure by listening to the speaker or looking at the recovery drive LED.
- Two beeps and the end of activity in the recovery drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery. In case of a BIOS recovery failure, verify that SPD memory is installed and retry the BIOS recovery procedure. If non-SPD memory is installed, replace with SPD memory and try the procedure again.

NOTE

BIOS recovery cannot be accomplished if non-SPD DIMMs are installed. The SPD data structure is required for the recovery process.

To create a BIOS recovery diskette or CD-ROM, a bootable LS-120 diskette or CD-ROM must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Upgrade Utility are available from Intel Customer Support through the Intel World Wide Web site.

NOTE

If the computer is configured to boot from an LS-120 diskette (in the Removable Devices submenu), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

For information about	Refer to
The BIOS recovery mode	Section 2.9, page 61
The Boot menu in the BIOS Setup program	Section 4.7, page 98
Contacting Intel customer support	Section 1.2, page 16

3.8 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The fourth device is disabled.

3.8.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot to the next defined drive.

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

For information about	Refer to
The El Torito specification	Section 1.3, page 16

3.8.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.9 Fast Booting Systems with Intel® Rapid BIOS Boot

Three factors affect system boot speed:

- Selecting and configuring peripherals properly
- Using an optimized BIOS, such as the Intel® Rapid BIOS
- Selecting a compatible operating system

3.9.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as “power-up to data ready” less than eight seconds, that minimize hard drive startup delays.
- Select a CD-ROM drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.
- Try different monitors. Some monitors initialize and communicate with the BIOS more quickly, which enables the system to boot more quickly.

3.9.2 Intel Rapid BIOS Boot

Use of the following BIOS Setup program settings reduces the POST execution time.

In the Boot Menu:

- Set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- Disable Quiet Boot, which eliminates display of the logo splash screen. This could save several seconds of painting complex graphic images and changing video modes.
- Enabled Intel Rapid BIOS Boot. This feature bypasses memory count and the search for a diskette drive

In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.

NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from 3 to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced Menu in the IDE Configuration Submenu of the BIOS Setup Program).

For information about	Refer to
IDE Configuration Submenu in the BIOS Setup Program	Section 4.4.4, page 90

3.9.3 Operating System

The Microsoft Windows Millennium Edition (Windows Me) operating system has built-in capabilities for making PCs boot more quickly. To speed operating system availability at boot time, limit the number of applications that load into the system tray or the task bar.

3.10 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 49 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 49. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options *	Can change all options *	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

* If no password is set, any user can change all Setup options.

For information about	Refer to
Setting user and supervisor passwords	Section 4.5, page 96

4 BIOS Setup Program

What This Chapter Contains

4.1 Introduction

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

```
Maintenance   Main   Advanced   Security   Power   Boot   Exit
```

Table 50 lists the BIOS Setup program menu functions.

Table 50. BIOS Setup Program Menu Functions

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and allows memory settings	Allocates resources for hardware components	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features	Selects boot options and power supply controls	Saves or discards changes to Setup program options

NOTE

In this chapter, all examples of the BIOS Setup Program menu bar include the maintenance menu; however, the maintenance menu is displayed only when the board is in configuration mode. Section 2.9 on page 61 tells how to put the board in configuration mode.

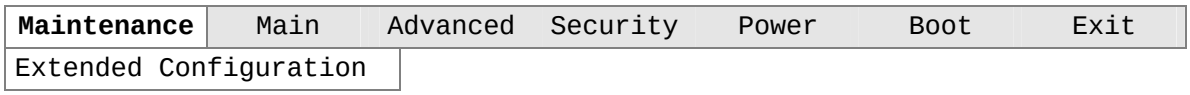
Table 51 lists the function keys available for menu screens.

Table 51. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen
<↑> or <↓>	Selects an item
<Tab>	Selects a field
<Enter>	Executes command or selects a submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

4.2 Maintenance Menu

To access this menu, select Maintenance on the menu bar at the top of the screen.



The menu shown in Table 52 is for clearing Setup passwords and enabling extended configuration mode. Setup only displays this menu in configuration mode. See Section 2.9 on page 61 for configuration mode setting information.

Table 52. Maintenance Menu

Feature	Options	Description
▸ Clear All Passwords	• **Yes (default)** • No	Selecting *Yes* clears all passwords.
▸ Clear BIS Credentials	• **Yes (default)** • No	Selecting *Yes* clears the WfM BIS (Boot Integrity Service) credentials.
▸ Extended Configuration	• **Default (default)** • User-Defined	Selecting *User-Defined* allows setting memory configuration.
CPU Information:		
CPU Microcode Update Revision	No options	Displays CPU's Microcode Update Revision.
CPU Stepping Signature	No options	Displays CPU's Stepping Signature.

4.2.1 Extended Configuration Submenu

To access this menu, select Maintenance on the menu bar, then Extended Configuration.

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Extended Configuration						

The submenu shown in Table 53 is for setting system memory configuration. This submenu becomes available when User-Defined is selected under Extended Configuration.

⚠ CAUTION

Choosing the wrong settings could cause system problems. Do not change these settings unless you have all the necessary information about the installed memory.

Table 53. Extended Configuration Submenu

Feature	Options	Description
Extended Configuration	**Default (default)** User-Defined	Selecting user-defined allows you to select *Default* or *User-Defined*. Selecting *User-Defined* allows you to configure the items listed under Memory Control below. Note: If *User-Defined* is selected, the status will be displayed in the Advanced Menu as: "Extended Menu: Used."
Memory Control:		
SDRAM Auto Configuration	• **Auto (default)** • User-Defined	Sets extended memory configuration options to auto or user-defined.
CAS# Latency	• 3 • 2 • **Auto (default)**	Selects the number of clock cycles required to address a column in memory.
SDRAM RAS# to CAS# delay	• 3 • 2 • **Auto (default)**	Selects the number of clock cycles between addressing a row and addressing a column.
SDRAM RAS# Precharge	• 3 • 2 • **Auto (default)**	Selects the length of time required before accessing a new row.

4.3 Main Menu

To access this menu, select Main on the menu bar at the top of the screen.

Maintenance	**Main**	Advanced	Security	Power	Boot	Exit

Table 54 describes the Main Menu. This menu reports processor and memory information and is for configuring the system date and system time.

Table 54. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS
Processor Type	No options	Displays processor type
Processor Speed	No options	Displays processor speed
Front Side Bus Speed	No options	Displays the system bus speed
Cache RAM	No options	Displays the size of second-level cache
Total Memory	No options	Displays the total installed SDRAM memory
Memory Bank 0 Memory Bank 1	No options No options	Displays *SDRAM* or *Not Installed* indicating the presence or absence of memory in Memory Banks 0 and 1
Language	• **English (default)** • Français • Portugues	Selects the current default language used by the BIOS
	•	
System Time	Hour, minute, and second	Specifies the current time
System Date	Month, day, and year	Specifies the current date

4.4 Advanced Menu

To access this menu, select Advanced on the menu bar at the top of the screen.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

Table 55 describes the Advanced Menu. This menu is used for setting advanced features that are available through the chipset.

Table 55. Advanced Menu

Feature	Options	Description
Extended Configuration	No options	If *Used* is displayed, *User-Defined* has been selected in Extended Configuration under the Maintenance Menu.
PCI Configuration	Select to display submenu	Configures individual PCI slot's IRQ priority. When selected, displays the PCI Configuration submenu.
Boot Configuration	Select to display submenu	Configures Plug and Play and the Numlock key, and resets configuration data. When selected, displays the Boot Configuration submenu.
Peripheral Configuration	Select to display submenu	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
IDE Configuration	Select to display submenu	Specifies type of connected IDE devices.
Diskette Configuration	Select to display submenu	When selected, displays the Diskette Configuration submenu.
Event Log Configuration	Select to display submenu	Configures Event Logging. When selected, displays the Event Log Configuration submenu.
Video Configuration	Select to display submenu	Configures video features. When selected, displays the Video Configuration submenu.

4.4.1 PCI Configuration Submenu

To access this submenu, select Advanced on the menu bar, then PCI Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 56 is for configuring the IRQ priority of PCI slots individually.

Table 56. PCI Configuration Submenu

Feature	Options	Description
PCI Slot 1 IRQ Priority	• **Auto (default)** 3 5 9 10 11	Allows selection of IRQ priority.
PCI Slot 2 IRQ Priority	• **Auto (default)** 3 5 9 10 11	Allows selection of IRQ priority.

4.4.2 Boot Configuration Submenu

To access this submenu, select Advanced on the menu bar, then Boot Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 57 is for setting Plug and Play options, resetting configuration data, and the power-on state of the Numlock key.

Table 57. Boot Configuration Submenu

Feature	Options	Description
Plug & Play O/S	• **No (default)** • Yes	Specifies if manual configuration is desired. *No* lets the BIOS configure all devices. This setting is appropriate when using a Plug and Play operating system. *Yes* lets the operating system configure Plug and Play devices not required to boot the system. This option is available for use during lab testing.
Reset Config Data	• **No (default)** • Yes	*No* does not clear the PCI/PnP configuration data stored in flash memory on the next boot. *Yes* clears the PCI/PnP configuration data stored in flash memory on the next boot.
Numlock	• Off • **On (default)**	Specifies the power-on state of the Numlock feature on the numeric keypad of the keyboard.

4.4.3 Peripheral Configuration Submenu

To access this submenu, select Advanced on the menu bar, then Peripheral Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 58 is used for configuring computer peripherals.

Table 58. Peripheral Configuration Submenu

Feature	Options	Description
Serial port A	• Disabled • Enabled • **Auto (default)**	Configures serial port A. *Auto* assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address (This feature is present only when Serial Port A is set to *Enabled*)	• **3F8 (default)** • 2F8 • 3E8 • 2E8	Specifies the base I/O address for serial port A, if serial port A is Enabled.
Interrupt (This feature is present only when Serial Port A is set to *Enabled*)	• IRQ 3 • **IRQ 4 (default)**	Specifies the interrupt for serial port A, if serial port A is Enabled.
Parallel port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • **Bi-directional (default)** • EPP • ECP	Selects the mode for the parallel port. Not available if the parallel port is disabled. *Output Only* operates in AT† -compatible mode. *Bi-directional* operates in PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bi-directional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode.

continued

Table 58. Peripheral Configuration Submenu (continued)

Feature	Options	Description
Base I/O address (This feature is present only when Parallel Port is set to *Enabled*)	• **378 (default)** • 278	Specifies the base I/O address for the parallel port.
Interrupt (This feature is present only when Parallel Port is set to *Enabled*)	• IRQ 5 • **IRQ 7 (default)**	Specifies the interrupt for the parallel port.
DMA (This feature is present only when Parallel Port Mode is set to *ECP*)	• 1 • **3 (default)**	Specifies the DMA channel.
Audio Device	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem.
LAN Device	• Disabled • **Enabled (default)**	Enables or disables the LAN device.
Legacy USB Support	• Disabled • **Enabled (default)**	Enables or disables USB legacy support. (See Section 3.5 on page 75 for more information.)

4.4.4 IDE Configuration Submenu

To access this submenu, select Advanced on the menu bar, then IDE Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The menu represented in Table 59 is used to configure IDE device options.

Table 59. IDE Configuration Submenu

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both (default)**	Specifies the integrated IDE controller. *Primary* enables only the primary IDE controller. *Secondary* enables only the secondary IDE controller. *Both* enables both IDE controllers.
Hard Disk Pre-Delay	• **Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay.
Primary IDE Master	Select to display sub-menu	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Primary IDE Slave	Select to display sub-menu	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master	Select to display sub-menu	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu.
Secondary IDE Slave	Select to display sub-menu	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.4.4.1 Primary/Secondary IDE Master/Slave Submenus

To access these submenus, select Advanced on the menu bar, then IDE Configuration and then the master or slave to be configured.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration **Primary IDE Master** **Primary IDE Slave** **Secondary IDE Master** **Secondary IDE Slave**
Diskette Configuration
Event Log Configuration
Video Configuration

There are four IDE submenus: primary master, primary slave, secondary master, and secondary slave. Table 60 shows the format of the IDE submenus. For brevity, only one example is shown.

Table 60. Primary/Secondary IDE Master/Slave Submenus

Feature	Options	Description
Drive Installed	No options	Displays the type of drive installed
Type	• None • User • **Auto (default)** • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. *User* allows capabilities to be changed. *Auto* fills-in capabilities from ATA/ATAPI device.
Maximum Capacity	No options	Displays the capacity of the drive.
LBA Mode Control	• Disabled • **Enabled (default)**	Enables or disables LBA mode control.
Multi-Sector Transfers	• **Disabled (default)** • 2 Sectors • 4 Sectors • 8 Sectors • 16 Sectors	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting.

continued

Table 60. Primary/Secondary IDE Master/Slave Submenus (continued)

Feature	Options	Description
PIO Mode	• **Auto (default)** • 0 • 1 • 2 • 3 • 4	Specifies the PIO mode.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4	Specifies the Ultra DMA mode for the drive.
Cable Detected	No options	Displays the type of cable connected to the IDE interface: 40-conductor or 80-conductor (for Ultra ATA-100 devices).

4.4.5 Diskette Configuration Submenu

To access this menu, select Advanced on the menu bar, then Diskette Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 61 is used for configuring the diskette drive.

Table 61. Diskette Configuration Submenu

Feature	Options	Description
Diskette Controller	• Disabled • **Enabled (default)**	Disables or enables the integrated diskette controller.
Floppy A	• Not Installed • 360 KB 5¼" • 1.2 MB 5¼" • 720 KB 3½" • **1.44/1.25 MB 3½" (default)** • 2.88 MB 3½"	Specifies the capacity and physical size of diskette drive A.
Diskette Write-Protect	• **Disabled (default)** • Enabled	Disables or enables write-protect for the diskette drive.

4.4.6 Event Log Configuration Submenu

To access this menu, select Advanced on the menu bar, then Event Log Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 62 is used to configure the event logging features.

Table 62. Event Log Configuration Submenu

Feature	Options	Description
Event log	No options	Indicates if there is space available in the event log.
Event log validity	No options	Indicates if the contents of the event log are valid.
View event log	[Enter]	Displays the event log.
Clear all event logs	• **No (default)** • Yes	Clears the event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of events.
Mark events as read	[Enter]	Marks all events as read.

4.4.7 Video Configuration Submenu

To access this menu, select Advanced on the menu bar, then Video Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 63 is for configuring the video features.

Table 63. Video Configuration Submenu

Feature	Options	Description
Primary Video Adapter	• **AGP (default)** • PCI	Selects primary video adapter to be used during boot.

4.5 Security Menu

To access this menu, select Security from the menu bar at the top of the screen.

Maintenance	Main	Advanced	**Security**	Power	Boot	Exit

The menu represented by Table 64 is for setting passwords and security features.

Table 64. Security Menu

Feature	Options	Description
Supervisor Password Is	No options	Reports if there is a supervisor password set.
User Password Is	No options	Reports if there is a user password set.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Clear User Password (Note 1)	• **Yes (default)** • No	Clears the user password.
User Access Level (Note 2)	• Limited • No Access • View Only • **Full (default)**	Sets BIOS Setup Utility access rights for user level.
Unattended Start (Note 1)	• **Disabled (default)** • Enabled	Enabled allows system to complete the boot process without a password. The keyboard remains locked until a password is entered. A password is required to boot from a diskette.

Notes:

1. This feature appears only if a user password has been set.
2. This feature appears only if a supervisor password has been set.

4.6 Power Menu

To access this menu, select Power from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit

The menu represented in Table 65 is for setting the power management features.

Table 65. Power Menu

Feature	Options	Description
Power Management (Note)	• Disabled • **Enabled (default)**	Enable or disable the BIOS power management feature.
Inactivity Timer (Note)	• Off • 1 Minute • 5 Minutes • 10 Minutes • **20 Minutes (default)** • 30 Minutes • 60 Minutes • 120 Minutes	Specifies the amount of time before the computer enters standby mode, when APM power management is active.
Hard Drive (Note)	• **Disabled (default)** • Enabled	Enables or disables power management for hard disks during standby and suspend modes, when APM power management is active.
ACPI Suspend State	• **S1 State (default)** • S3 State	Specifies the ACPI suspend state.
Power Button Mode	• **On/Off (default)** • Suspend	Selects the operating mode for the power button.

Note: Power Management, Inactivity Timer, and Hard Drive features apply only for APM operating systems.

4.7 Boot Menu

To access this menu, select Boot from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					IDE Drive Configuration	

The menu represented in Table 66 is used to set the boot features and the boot sequence.

Table 66. Boot Menu

Feature	Options	Description
Silent Boot	• Disabled • **Enabled (default)**	*Disabled* displays normal POST messages. *Enabled* displays OEM graphic instead of POST messages.
Intel Rapid BIOS Boot	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
After Power Failure	• Stays Off • **Last State (default)** • Power On	Specifies the mode of operation if an AC power loss occurs. *Stay Off* keeps the power off until the power button is pressed. *Last State* restores the previous power state before power loss occurred. *Power On* restores power to the computer.
Wake on Modem Ring	• **Stay Off (default)** • Power On	In APM mode only, specifies how the computer responds to an incoming call on an installed modem when the power is off.
Wake on LAN	• **Stay Off (default)** • Power On	In APM mode only, determines how the system responds to a LAN wake up event.
Wake on PME	• **Stay Off (default)** • Power On	In APM mode only, determines how the system responds to a PCI power management event.

continued

Table 66. Boot Menu (continued)

Feature	Options	Description
1st Boot Device 2nd Boot Device 3rd Boot Device 4th Boot Device	• Floppy • ARMD-FDD (Note 1) • ARMD-HDD (Note 2) • IDE-HDD (Note 3) • ATAPI CDROM • Intel UNDI, PXE 2.0 (Note 4) • Disabled	Specifies the boot sequence according to the device type. The computer will attempt to boot from up to four devices as specified here. Only one of the devices can be an IDE hard disk drive. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device. The default settings for the first through fourth boot devices are, respectively: • Floppy • IDE-HDD • ATAPI CDROM • Disabled ***NOTE:*** *To configure the computer to boot from an IDE hard disk drive, set a boot device in the Setup feature to* IDE-HDD*. Determine the IDE channel, and master or slave mode of the drive. Then, in the next Setup feature,* IDE Drive Configuration*, set that channel and mode to* 1st IDE*.*
▸ IDE Drive Configuration Primary Master IDE Primary Slave IDE Secondary Master IDE Secondary Slave IDE	• **1st IDE (default)** • 2nd IDE • 3rd IDE • 4th IDE	*1st IDE* specifies the IDE hard disk drive to boot from. The *2nd* through *4th IDE* settings are ignored. See the note above for more information. To specify the drive to boot from: 1. Use <↑> or <↓> to select the channel, and master or slave mode of the drive to boot from. 2. Press <Enter>. 3. Use <↑> or <↓> to select 1st IDE. 4. Press <Enter> to set the selection.

Notes:

1 ARMD-FDD = ATAPI removable device - floppy disk drive

2 ARMD-HDD = ATAPI removable device - hard disk drive

3 HDD = Hard Disk Drive

4 This boot device is available only when the onboard LAN subsystem is present.

4.8 Exit Menu

Maintenance	Main	Advanced	Security	Power	Boot	**Exit**

The menu represented in Table 67 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

Table 67. Exit Menu

Feature	Description
▸ Exit Saving Changes	Exits and saves the changes in CMOS SRAM.
▸ Exit Discarding Changes	Exits without saving any changes made in the BIOS Setup program.
▸ Load Setup Defaults	Loads the factory default values for all the Setup options.
▸ Load Custom Defaults	Loads the custom defaults for Setup options.
▸ Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
▸ Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

What This Chapter Contains

5.1 BIOS Error Messages

Table 68 lists the error messages and provides a brief description of each.

Table 68. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate-A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive - ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible Sec Master Drive - ATAPI Incompatible Sec Slave Drive - ATAPI Incompatible	Corresponding drive is not an ATAPI device. Run Setup to make sure device is selected correctly.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
HDC Failure	Error occurred trying to access hard disk controller.

continued

Table 68. BIOS Error Messages (continued)

Error Message	Explanation
Checking NVRAM.....	NVRAM is being checked to see if it is valid.
Update OK!	NVRAM was invalid and has been updated.
Updated Failed	NVRAM was invalid but was unable to be updated.
Keyboard Is Locked	The system keyboard lock is engaged. The system must be unlocked to continue to boot.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed, then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added, there may be a problem with the system.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed, then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an offboard card. This error is followed by an address.
On Board Parity Error	A parity error occurred in onboard memory. This error is followed by an address.
Parity Error	A parity error occurred in onboard memory at an unknown address.
NVRAM / CMOS / PASSWORD cleared by Jumper	NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 69 defines the Uncompressed INIT Code Checkpoints, Table 70 describes the Boot Block Recovery Code Check Points, and Table 71 lists the Runtime Code Uncompressed in F000 Shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 69. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Do necessary chipset initialization, start memory refresh, do memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If the BIOS is in recovery mode or the main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find Main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 70. Boot Block Recovery Code Check Points

Code	Description of POST Operation
E0	Onboard floppy controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller, interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize ATAPI CD-ROM drive.
EA	Try to boot from ATAPI CD-ROM. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS-120, ZIP†) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from ATAPI CD-ROM failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Table 71. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23, 24 blocking/unblocking command.
11	Going to check pressing of <INS>, <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, output devices) to start if present. (See Section 5.3 for details of different buses.)
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate display memory R/W test.
32	Alternate display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power on message.
38	Different buses init (input, IPL, general devices) to start if present. (See Section 5.3 for details of different buses.)
39	Display different buses initialization error messages. (See Section 5.3 for details of different buses.)
3A	New cursor position read and saved. To display the Hit <DEL> message.

continued

Table 71. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640 K memory.
48	Patterns written in base memory. Going to find out amount of memory below 1 M memory.
49	Amount of memory below 1 M found and verified. Going to find out amount of memory above 1 M memory.
4B	Amount of memory above 1 M found and verified. Check for soft reset and going to clear memory below 1 M for soft reset. (If power on, go to check point # 4Eh).
4C	Memory below 1 M cleared. (SOFT RESET) Going to clear memory above 1 M.
4D	Memory above 1 M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64 K memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1 M complete. Going to adjust displayed memory size for relocation/ shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1 M to follow.
52	Memory testing/initialization above 1 M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.

continued

Table 71. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done.
91	Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start. (See Section 5.3 for details of different buses.)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area.
9A	Return after setting timer. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test.
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after coprocessor test.
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID, and Num Lock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	Put INT13 module runtime image to shadow.
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in Shadow.

continued

Table 71. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT19 boot loader.

5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 72 describes the bus initialization checkpoints.

Table 72. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, and general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 73 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 73. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on the bus concerned
1	func#1, static devices init on the bus concerned
2	func#2, output device init on the bus concerned
3	func#3, input device init on the bus concerned
4	func#4, IPL device init on the bus concerned
5	func#5, general device init on the bus concerned
6	func#6, error reporting for the bus concerned
7	func#7, add-on ROM init for all buses

Table 74 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 74. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	Onboard system devices
2	ISA devices (not supported)
3	EISA devices (not supported)
4	ISA PnP devices (not supported)
5	PCI devices

5.4 Speaker

A 47 Ω inductive speaker is mounted on the D810E2CB board. The speaker provides audible error code (beep code) information during the power-on self-test (POST).

For information about	Refer to
The location of the onboard speaker	Figure 1, page 14

5.5 BIOS Beep Codes

Whenever a recoverable error occurs during power-on self-test (POST), the BIOS displays an error message describing the problem (see Table 75). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 75. Beep Codes

Beep	Description
1	Refresh failure
2	Parity cannot be reset
3	First 64 KB memory failure
4	Timer not operational
5	Not used
6	8042 GateA20 cannot be toggled
7	Exception interrupt error
8	Display memory R/W error
9	Not used
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g., POST module not found, etc.)